SIEMENS

Data Book 1976/77

MOS-Circuits

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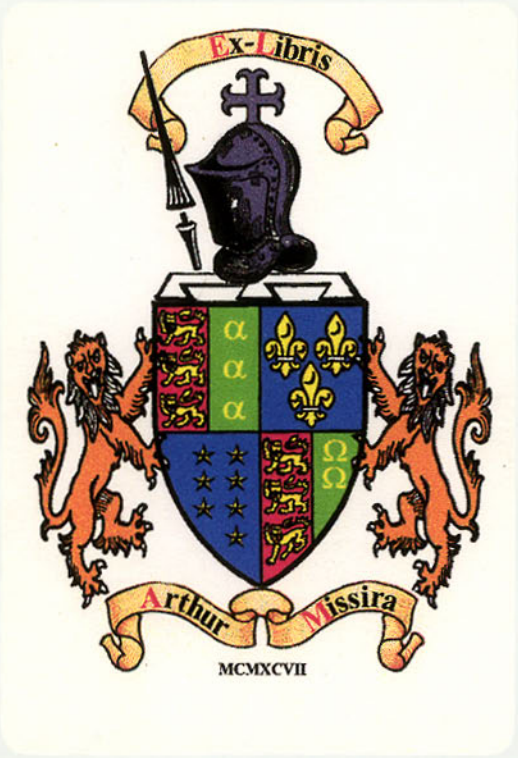

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4. MOS-circuits for industrial applications

1. General Information on MOS-Circuits

1.1. Introduction to the MOS technology

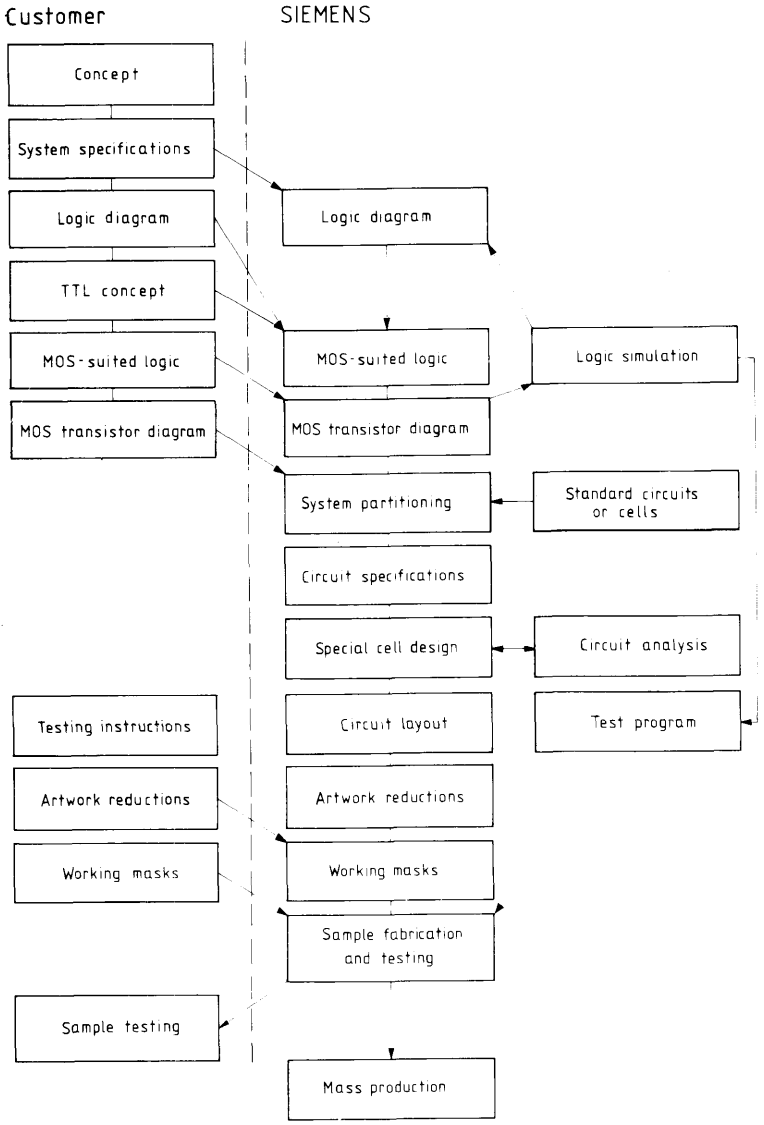
MOS is a technology used for the fabrication of largescale integratet digital circuits.
MOS is the abbreviation of **M**etal-**O**xide-**S**ilicon, which also explains the principle construction of a transistor (see fabrication of the MOS-transistor, page 11).

The main advantages of the MOS technology are:

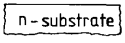
- simple construction of the transistors
- high density of integration
- extremely low power consumption of the transistors

On a silicon chip with an area of no more than 30 mm^2, up to 20 000 transistors can be integrated today. By 1980 it will be possible to realize 100 000 transistors on a single chip. The increasing level of integration causes a growing proportion of the development- and fabrication-value to be shifted from the equipment manufacturer to the component manufacturer. Siemens, as a component manufacturer, offers her customers the chance of a joint development of application-specific MOS-circuits, in addition to supplying standard circuits. There is also a possibility of Siemens second-sourcing a specific circuit already used by the customer. A requirement for this is the compatibility of technology.
The diagram on page 10 shows, at which development steps of an MOS project a cooperation between the customer and Siemens is possible.

Possible cooperation of Siemens with the customer at the various stages of an MOS-circuit development

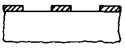


1.2 Fabrication of the MOS transistor (p-channel)



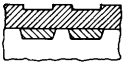
Starting material: n-conducting silicon

Growing a layer of silicon-oxide (0,5 μm)



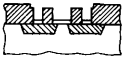
Using photo-lithography and a first mask, windows for the p-regions source and drain are produced.

Diffusion of the p-regions



Deposition of a layer of thick oxide (1,2 μm)

Using the second mask, windows for the three contacts are etched



Growing the gate oxide (0,1 μm)

Removal of the gate oxide covering the source and drain regions by means of a third masking step

Vapor deposition of aluminum as contact- and interconnect-metal (fourth masking step)

Using a final fifth mask, the connection pads used for bonding are exposed.

1.3. MOS fabrication processes

Basic differences of the various fabrication techniques can be found in the construction of the gates and the type of doping of the substrate. The gate electrodes of the transistors are made either with aluminum metal or silicon. Therefore, these techniques are called *Metal-Gate technique* or *Silicon-Gate-technique*, respectively. Until 1975, n-type substrate material was used in all fabrication processes. Consequently, the resulting transistor channels were of the p-type and this process was called *p-channel process*. The counterpart is the *n-channel process*. Both processes will be explained in the following paragraphs.

A further distinguishing characteristic is the state of conduction of the integrated transistors. Without a voltage applied to the gate, a transistor may be conducting or non-conducting.

If conducting, it is called a depletion transistor. This means that an increasing voltage applied between gate and source will tend to narrow-down the channel by gradually depleting it of charge carriers. The resistance of the conducting path rises from a typical value of about 10 kΩ to 10^{15} Ω. This mode of operation is called "depletion mode". The opposite occurs with a transistor of the so-called enhancement type. In this type of transistor the conductive channel is formed and enhanced by an increase of the gate-source voltage. Therefore, this mode of operation is called "enhancement mode".
A channel is a conducting path between source and drain, caused by a charge inversion in the upper layer of the substrate, underneath the gate oxide. This inversion usually involves a depth of about 10nm, equal to 100 Angström. The inversion layer is p-conducting for the p-channel process and n-conducting for the n-channel process.

1.3.1. Metal-gate-technologies

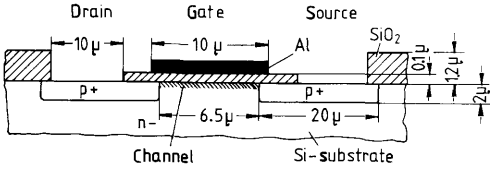
p-channel high-voltage-process

This process still remains to be the standard process. Its main advantages are the simplicity of the process and the resulting relatively low fabrication costs.

The process, which has been used for production since 1967, is very well controlled by the manufacturers with respect to yield and reliability. The high supply voltages result in a high noise immunity, which is of great benefit especially to custom circuits in industrial applications.

For standard circuits, the high supply voltage constitutes a disadvantage because the circuits are not compatible with bipolar circuit families.

The MOS-standard-process uses metal-gates and therefore is one of the so-called metal-gate-processes. It is predominantly used for custom logic circuits.



Standard-p-channel process

p-channel low-voltage-process

It has resulted from continued development of the high voltage-process by using additional ion-implantation steps to achieve low threshold voltages. So far, main application has been in metal-gate-processes.
The ion-implantation technique with depletion mode transistors offers a wide range of application possibilities. It is very flexible and can be used in most processes as an additional step.
The simultaneous use of conducting and non-conducting transistors on the same crystal (when the gate potential is equal to the source potential) results in circuits which are faster and have a considerably lower power requirement (about 1/10th of equivalent MOS-standard-circuits). They operate from only one supply voltage and offer a higher logic noise immunity.
Low punch-through voltages can be avoided.
The depletion-mode transistors, which function as current sources, are particularly suited to be used as integrated load transistors. They are capable of charging capacitive loads with a nearly linear charging characteristic.

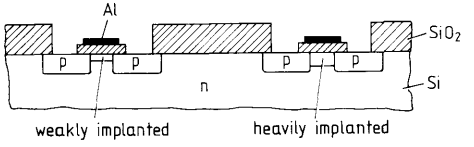
1. General Information on MOS-Circuits

The chip-internal processing of logic signals takes place at uniform logic levels, as only one supply voltage is used. This feature is important, because the logic circuit can be made smaller and chip area is saved. For example, an integrated four-input gate with ion-implantation consumes less than half the area it would need with the MOS-standard-process.

If the application requires, ion-implantation permits the design of circuits which work over a wide range of supply voltages. All other MOS-technologies require supply voltage tolerances of only ± 10%. However, this advantage must be paid for by a larger chip area than would be required otherwise. Ion-implantation can also be used in order to convert the high-voltage standard process to a low-voltage process. This is done by adding a process step in which ions of a particular concentration and depth of penetration are implanted into the channel area.

Threshold voltages of 3.5-4 V are thereby reduced to about 1.8-2 V. This means that the supply voltage of typically 24 V may be reduced to 8-10 V. This technique offers the advantage that with unchanged design rules already available basic cells, existing masks and the usual standard process can be used.

Fabrication processes using ion-implantation are very flexible and therefore particularly suited for the development and fabrication of custom circuits, which must be tailored to the requirements of a specific application.

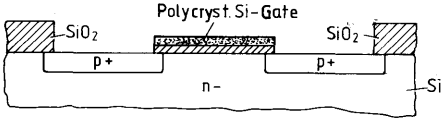


Ion-implantation
with depletion-mode

1.3.2 Silicon-gate-technologies

These technologies are called "selfaligning" because of a special gate-selfaligning feature of the fabrication process.

They constitute advanced technologies which are mainly used for the production of memories.



Silicon-gate-process

p-channel process

The fabrication process differs from the standard MOS-process in many ways. For instance, the control-electrode (gate) is made of silicon and fabricated before the drain- and source-diffusion step. Hence, the gate will function as a mask for the channel area, when the drain-and source-regions are diffused, thereby largely preventing an overlapping of the gate with these regions. (Overlaps result in unwanted parasitic capacitances which reduce the operating speed and increase the power dissipation). However, overlapping cannot be avoided entirely in the above process because of a horizontal diffusion, slightly undercutting the gate region.

The main applications of the process are for Random-Access-Memories, Read-Only-Memories and shift-registers, circuits with very regular structures. The smaller component structures on the crystal, resulting from the selfaligning feature of this process and the availability of the silicon-gate electrode as a third level of conductors, result in a higher density of integration than is possible with the metal-gate process.

The Si-gate process offers the user low supply voltage requirements (+5 V, −12 V).

Except for the additional −12 V supply voltage needed, silicon gate circuits are fully TTL-compatible. This means that the MOS-outputs can drive TTL-inputs directly and vice versa, and that the same clock generators may be used. TTL circuits may be driven directly.

n-channel process.

This process is the counterpart of the p-channel process. Having been an aluminum-gate process originally, it is now changing to be predominantly of the silicon-gate type; most n-channel circuits produced in the future will feature silicon gates. The construction of the transistors is the same, except for a different type of doping being used. While source and drain are produced through n-diffusion, the substrate consists of p-type silicon.

The physical properties of n-type silicon offer a three times better conductivity of the channel compared to p-MOS. A considerably higher switching speed results.

In the fabrication process, already minute quantities of impurities in the oxide cause very large changes in the threshold voltage. An absolutely clean environment is therefore an unconditional prerequisite for the fabrication area.

An improvement of the threshold voltage stability can be achieved through the application of an additional ion-implantation step.

Todays upper frequency limits of 10 to 20 MHz can be raised to a range of 50 to 100 MHz through the use of ion-implantation.

Because of a better noise margin and higher substrate doping level, a smaller spacing of the diffusion zones becomes tolerable. This results in a density of integration which, compared to the p-channel process, is about 50% higher.

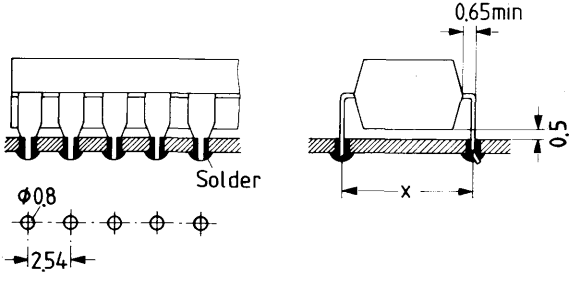
A further advantage is the use of only one supply voltage, 5 V, which makes this process fully compatible with TTL. Besides special logic circuits with high speed requirements (e. g. microprocessors), fast and highly integrated memories will be a preferred area of application of this technology in the future.

1.4. Mounting instructions

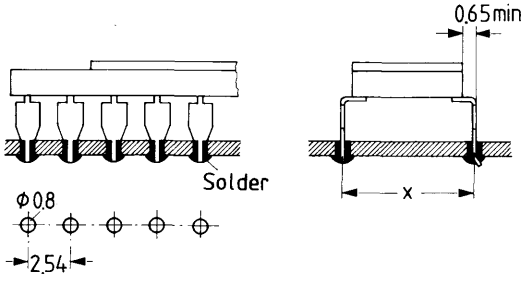
1.4.1. Plastic and ceramic plug-in packages

The packages are soldered on the reverse side of the printed circuit board, opposite the package. The package pins are bent 90° down and fit into holes 2.54 mm apart, with hole diameters of 0.7 to 0.9 mm. Dimension X should be taken from the appropriate dimensional drawing of the package.
The bottom of the package does not touch the printed circuit board surface after its insertion, as the pins widen at a proper distance from the package (see figure).

After inserting the package into the printed circuit board it is advantageous to bend two pins at an angle of approximately 30° relative to the board. This way the package does not need to be held down during the soldering process. The maximum allowable solder temperature for iron soldering is 265°C (maximum 10 s) and for dip soldering 240°C (max. 4 s).



Plastic plug-in package



Ceramic plug-in package

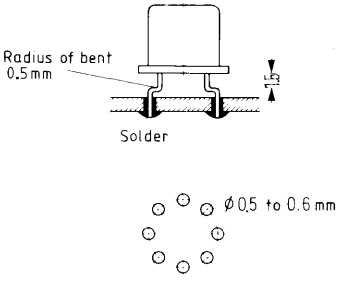
1.4.2. Package 5 H8 DIN 41873 and similar packages with 8, 10 and 12 pins.

The position of the case is arbitrary. The pins may be bent sideways at a minimum distance of 1.5 mm from the case according to the hole distance. Pins that are too long should be clipped before soldering.

Iron- or dip-soldering may be used.

The maximum solder times are, for dip soldering, t_{max} = 5 s for 250°C solder temperature
t_{max} = 4 s for 300°C solder temperature

and for iron soldering t_{max} = 15 s for 250°C solder temperature
t_{max} = 12 s for 300°C solder temperature



1.5. Protection measures for MOS-circuits

To guard the sensitive MOS-circuits against destructive static overvoltages and electrical spikes, protection devices have been integrated into the chips at all inputs and outputs:

1. In the case of positive overvoltages, a pn-junction becomes conducting in foreward direction, to substrate.
2. Negative overvoltages cause a defined diode-breakdown with current limiting.
3. In addition, all inputs and outputs are connected to the gate and drain of a transistor with a turn-on voltage of −35 V; these transistors will short-circuit inputs or outputs subjected to overvoltages.

In spite of these protective measures it should be considered however, that floors of a plastic material, non-conducting working surfaces and chairs, as well as work-clothes made of synthetic materials could cause a built-up of charges which might become dangerous for the circuits.
Machines and tools getting in contact with MOS circuits must be kept on the same potential as these. In addition, the working surfaces and the persons handling MOS circuits should be kept on this potential.
As an additional protective measure to reduce static charges, a relative humidity of about 70% in the air of the fabrication rooms will be advantageous.

If automatic handling is used, an air-ionizer is recommended for the prevention of static charge built-up.

When MOS-circuits are installed in the equipment, maximum ratings should be carefully observed. A high-resistance grounding of the dip-solder or soldering-iron is mandatory. In the case of dip-soldering, care should be taken that excessive voltage differences are avoided.
p(n)-channel MOS-circuits must not be subjected to positive (negative) voltages at their pins relative to the substrate potential V_{SS}.

Protective measures for the electrical operation

If noise voltages can happen to occur during the electrical operation of MOS circuits and reach the pins, care should be taken that the maximum ratings of the voltage levels are not exceeded. In particular, it is advisable that the supply voltages V_{DD}-V_{SS} or V_{GG}-V_{SS}, respectively, are shunted right close to the circuit by a capacitor with a low impedance for high frequencies.

Noise voltages which could reach positive values with respect to V_{SS}, must be limited by an appropriate diode-circuit.

MOS-circuits are not to be plugged into their sockets or unplugged while voltage is being applied.

1.6. Type nomenclature for MOS-circuits

For MOS-circuits two types of nomenclature are being used:

1.6.1. Siemens nomenclature

MOS standard circuits intended for a narrow range of applications are designated by S and a 3-digit number.

1.6.2. PRO ELECTRON nomenclature

For MOS standard circuits intended for a wide range of applications the PRO ELECTRON code is used.

1) New PRO ELECTRON code (in use since 1973).

The code consists of **three letters** followed by a **serial number.**

First two letters

A. Solitary circuits

The first letter identifies the circuit as an

S: solitary digital circuit
T: analog circuit
U: mixed analog/digital circuit

The **second letter** has no fixed significance, with the exception of the letter H designating a hybrid circuit.

B. Family circuits

are digital integrated circuits related in their specifications and designed to be mutually connected.

The **first two letter** identify the **family.**

The **third letter** indicates the operating temperature or in exceptional cases another characteristic.

A –	no temperature range specified	
B –	0 to + 70 °C	If a circuit has been designed for a wider temperature range but does not yet qualify for a higher classification, the code letter for the narrower temparature range is used.
C –	−55 to +125 °C	
D –	−25 to + 70 °C	
E –	−25 to + 85 °C	
F –	−40 to + 85 °C	

The serial number may either be a 4-digit number (assigned by **PRO ELECTRON)** or the serial number (combining figures and perhaps numbers) of an existing company number. Company numbers consisting of less than four digits are extended to a four-digit number by adding zeroes (0) in front.

A version-letter may be added to indicate a variation of the basic type.

The following letters are recommended for package variations:

C: cylindrical package
D: dual in-line
F: flat pack
Q: quadruple in-line

For other variants, the letters have no fixed significance with the exception of the letter Z: Internal connection as specified by customer ("customized wiring").

2) Former PRO ELECTRON-code

First two letters: same as new code
The third letter: indicates the function

H – Combinatorial circuit
J – Bistable or multistable sequential circuit
K – Monostable sequential circuit
L – Level converter
N – Bi-metastable or multistable sequential circuit
Q – Read-write memory
R – Read-only memory
S – Sense amplifier with digital output
Y – Miscellaneous circuits not covered by H through S

The **third digit** (of the serial number of three digits) indicates the operating temperature range.

0 – No temperature range specified
1 – 0 to + 70°C
2 – −55 to +125°C
3 – −10 to +85°C
4 – +15 to +55°C
5 – −25 to +70°C
6 – −40 to +85°C

1.7. Quality data for MOS-circuits

1.7.1. Warranty

If incoming testing shows that the AQL (Acceptable Quality Level) figures are exceeded, the customer is entitled to refuse acceptance and demand replacement of the shipment received.

1.7.2. AQL-figures

The AQL-figures define the maximum number of defective components up to which a shipment received must be accepted.

	Application area		
Electrical defects	Industrial	Consumer	Entertainment
Single AQL, gradual electrical defects (1)	1.5	2.5	2.5
Single AQL, critical electrical defects (2)	0.4	0.65	0.65
Σ AQL, electrical defects	1.5	2.5	2.5
Mechanical defects			
Single AQL, gradual mechanical defects (3)	1.5	2.5	2.5
Single AQL, critical mechanical defects (4)	0.25	0.4	0.4
Σ AQL, mechanical defects	1.5	2.5	2.5

Breakdown of defects

ad 1: Defects affecting the function in a minor way (electrical data too low or too high).
ad 2: Catastrophic failures (no function, short circuits between the pins) and defects seriously limiting the function (falling below specified limits by more than 50%).
ad 3: Slight mechanical defects (missing type-marking, marking difficult to identify, wrong dimensions, heavy stamping-burrs at the pins, bent pins).
ad 4: Catastrophic failures (broken or cracked packages, wrong type-marking, wrong position of the package-nose or marking of pin 1, pins not solderable).

1.7.3. Receiving quality

The figures shown in the table are warranty-figures. However, the average outgoing quality (AOQ) of shipments is considerably higher, i.e. the proportion of defective components is much smaller than indicated by the AQL-figures.

1.7.4. Random sample testing

The AQL-figures are warranted for tests in accordance with random sampling test plan MIL Std. 105 D inspection level II.

1.7.5. Rejections

Returned IC's can be accepted only if the faulty samples are included in the rejected shipment.

1.7.6. AQL random sampling test plan

Random sampling test plan for normal inspection (MIL-Std. 105D, inspection level II)

Lot-size	Sample size	0.065		0.10		0.15		0.25		0.40		0.65		1.0		1.5		2.5		4.0		6.5	
		Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re
2 to 8	2																			↓		0	1
9 to 15	3																	↓		0	1	↕	
16 to 25	5															↓		0	1	↑		↕	
26 to 50	8															0	1	↑		↓		1	2
51 to 90	13													0	1	↑		↕		1	2	2	3
91 to 150	20											0	1	↑		↕		1	2	2	3	3	4
151 to 280	32									0	1	↑		↑		1	2	2	3	3	4	5	6
281 to 500	50							0	1	↕		↕		1	2	2	3	3	4	5	6	7	8
501 to 1200	80					0	1	↑		↕		1	2	2	3	3	4	5	6	7	8	10	11
1201 to 3200	125			0	1	↕		↑		1	2	2	3	3	4	5	6	7	8	10	11	14	15
3201 to 10000	200	0	1	↑		↕		1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22
10001 to 35000	315	↑		↕		1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	↑	
35001–150000	500	↓		1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	↑		↑	
150001–500000	800	1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	↑		↑		↑	
500001 and more	1250	2	3	3	4	5	6	7	8	10	11	14	15	21	22	↑		↑		↑		↑	

Ac = permissible number of defective sample elements; lot accepted
Re = excessive number of defective sample elements: lot rejected

Additional requirement:

As the combination "acceptance 0 and rejection 1" has a low degree of significance, the next larger sample size is to be used. All deliveries are subject to the „Allgemeine Verkaufsbedingungen für Erzeugnisse und Leistungen der Elektroindustrie" (General Sales Conditions for Products and Performances of the Electrotechnical Industry), and the „Allgemeine Lieferbedingungen für Erzeugnisse und Leistungen der Elektroindustrie" (General Delivery Conditions for Products and Performances of the Electrotechnical Industry).

1.8. Glossary of abbreviations used for MOS-circuits

Voltages

V	Voltage, general
V_{CC}	Supply voltage
V_{SS}	Substrate supply voltage
V_{DD}	Drain supply voltage
V_{GG}	Gate supply voltage
V_{IH}	High level at a signal input
V_{IL}	Low level at a signal input
V_{QH}	High level at an output
V_{QL}	Low level at an output
$V_{\phi H}$	High level at a clock input
$V_{\phi L}$	Low level at a clock input
V_I	Voltage at a signal input
V_R	Reset voltage

Currents

I_{DD}	Drain supply current
I_{GG}	Gate supply current
I_Q	Output current, general

Resistances

R_{QH}	High level output resistance
R_{QL}	Low level output resistance
R_Q	Load resistance at an output
R_I	Input resistance at a signal input
R_ϕ	Input resistance at a clock input
R	Resistance

Capacitances

C	Capacitance
C_I	Input capacitance
C_ϕ	Input capacitance at a clock input
C_Q	Output load capacitance

Frequencies

f_I	Input frequency
f_Φ	Clock frequency

Power

P	Power dissipation (power consumption)
P_{tot}	Power dissipation

Temperatures

T_{amb}	Ambient temperature
T_S	Storage temperature

Timing

t_d	Delay time
t_{pd}	Propagation delay
t_r	Rise time
t_f	Fall time
t_t	Transition time
t_w	Pulse width
t_{tHLQ}	Transition time HL of the output signal
t_{tLHQ}	Transition time LH of the output signal
t_{dHLQ}	Delay of the HL transition of the output signal
t_{dLHQ}	Delay of the LH transition of the output signal
$t_{wH\Phi}$	Pulse width at the H-level of the clock signal
$t_{wL\Phi}$	Pulse width at the L-level of the clock signal
$t_{tHL\Phi}$	HL transition time of the clock signal
$t_{tLH\Phi}$	LH transition time of the clock signal
$t_{dHL\Phi}$	Delay of the HL transition of the clock signal
$t_{dLH\Phi}$	Delay of the LH transition of the clock signal
t_{wHI}	Pulse width at the high level of the input signal
t_{wLI}	Pulse width at the low level of the input signal
t_{tHLI}	HL transition of the input signal
t_{tLHI}	LH transition of the input signal
t_{dLH}	Delay of the LH transition
t_{wHQ}	Pulse width at the high level of the output signal

Miscellaneous

Φ	Clock input
I	Input
I_1	Input 1
I_2	Input 2
$\underline{Q}$	Data output
$\overline{Q}$	Data output inverted

MOS-Circuits for Entertainment Applications

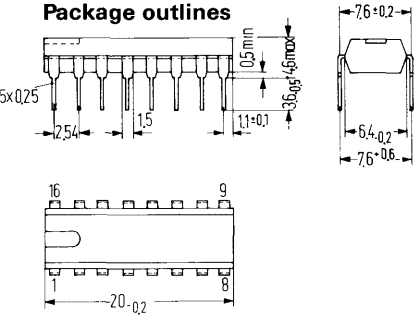
Type	Ordering code
S175 A	Q67100-Z58

This circuit is used for the control of three analog functions. It is suited for an application in TV remote control systems as well as for the control of speed and turning direction of dc-motors or other direct current consuming equipment, when used with the proper external circuitry.

The circuit contains a reference oscillator with dividers and three 6-bit up-and-down-counters with following D/A-converters. The counters are operated through their corresponding inputs. The stepping frequency can be doubled by applying an L-level at FU. This makes a regulation time between 4s and 16s possible, depending on the type of application. When the voltage is turned on the counters are automatically reset to a preprogrammed position; two memories into a middle position, one to 33% of the maximum value.

In order to enable power-saving standby-operation, the circuit can be operated from two supply voltages. With a turned-off supply voltage V_{SS} = OV and V_{GG} applied, the memory contents can be changed.

Package outlines



Plastic plug-in package
(16 pins DIL)
20 A 16 DIN 41866
Weight approx. 1.2 g

Pin connections

Pin-No	Designation	Function
1	V_{SS}	Operational supply voltage 1
2	C_1	Frequency setting 1
3	FU	Frequency switching
4	PU	Test pin
5	RI_1	Reset input 1
6	VI_1	Upcount input 1
7	RI_2	Downcount input 2
8	V_{DD}	Ground
9	V_{GG}	Operational supply voltage 2
10	VI_2	Upcount input 2
11	Q_1	Output 1
12	Q_2	Output 2
13	Q_3	Output 3
14	VI_3	Upcount input 3
15	RI_3	Downcount input 3
16	C_2	Frequency setting 2

Maximum ratings

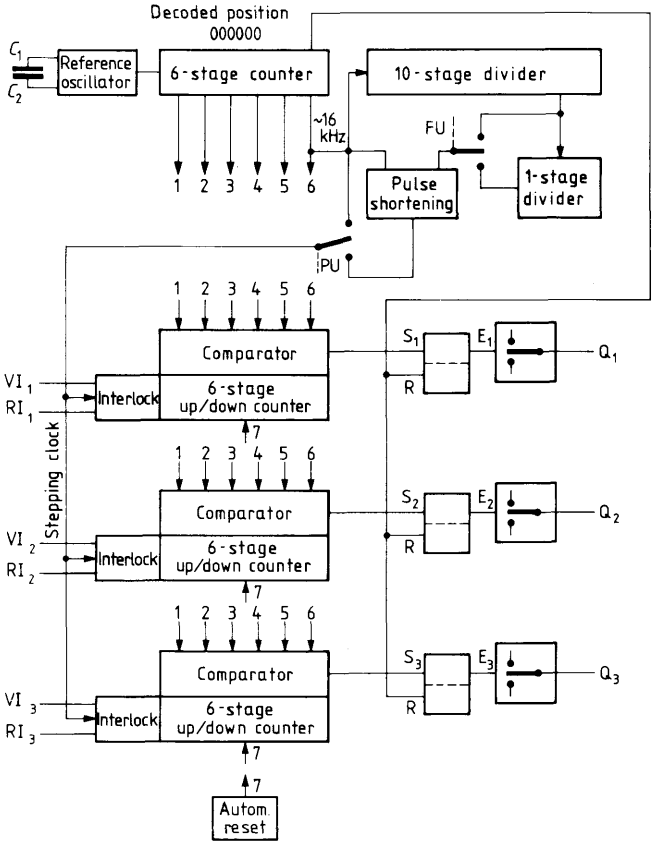
		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{SS}	1)	−0.3	17	V
	V_{ss}	2)	−0.3	7	V
	V_{GG}	2)	−15	0.3	V
Input voltage	V_I	1) + 2)	0	V_{SS}	V
Power dissipation	P_{tot}	1)		300	mW
		2)		200	mW
Ambient operating temperature	T_{amb}	1) + 2)	0	+60	°C
Storage temperature	T_S	1) + 2)	−55	+125	°C

Operating characteristics

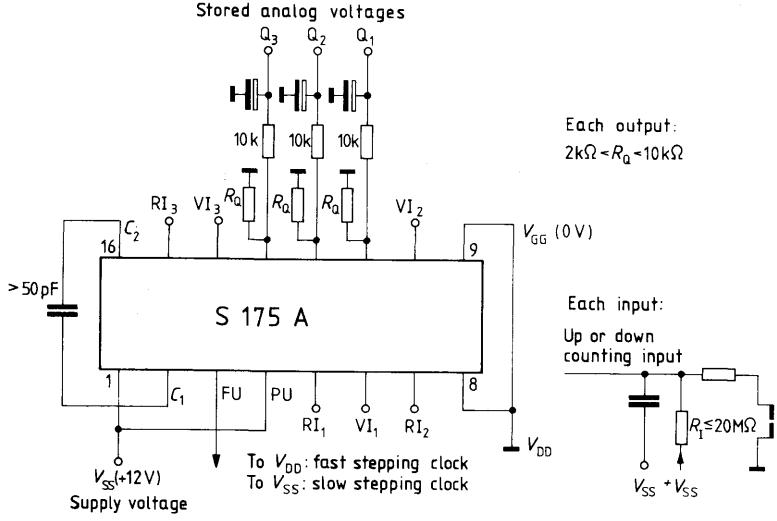
		Test condition	Lower limit B	Upper limit A	Unit
Supply voltages	V_{CC}	1)	9	13	V
	V_{CC}	2)	5.3	6.2	V
	V_{GG}	2)	−15	−10	V
Supply currents	I_{CC}	1)		20	mA
	I_{CC}	2)		20	mA
	I_{GG}	2)		400	µA
H-input voltage	V_{IH}	1) + 2)	V_{SS} = −0.5	V_{SS}	V
L-input voltage	V_{IL}	1)		4	V
		2)		1.5	V
Input resistance of the memory inputs	R_I	1)	5		MΩ
		2)	10		MΩ
Input resistance of input FU	R_I	1) + 2)	1		MΩ
L-output level	V_{QL}	1) + open output	0	1	V
H-output level	V_{QH}	1) + open output	V_{SS} = −1	V_{SS}	V
L-output level	V_{QL}	2) + open output	0	0.5	V
H-output level	V_{QH}	2) + open output	V_{SS} = −0.5	V_{SS}	V
Differential internal resistance	R_Q			1	kΩ
Short circuit current to ground or V_{CC}	I_Q	1)		|30|	mA
	I_Q	2)		|20|	mA

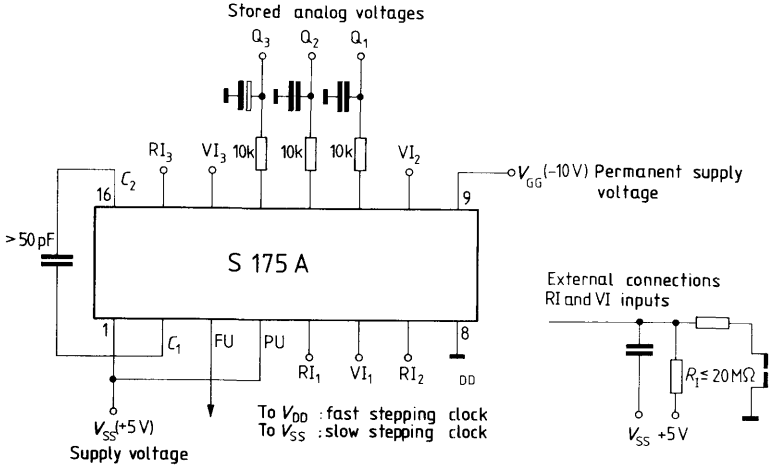
1) Pin 9 connected to pin 8 V_{GG} = 0 V
2) Power saving two voltage operation

Block diagram



External connections of the S 175 A





Message-Decoder for FM Road Traffic Information Service

S 551

Preliminary data

Type	Ordering code
S 551	Q 67100-Z 109

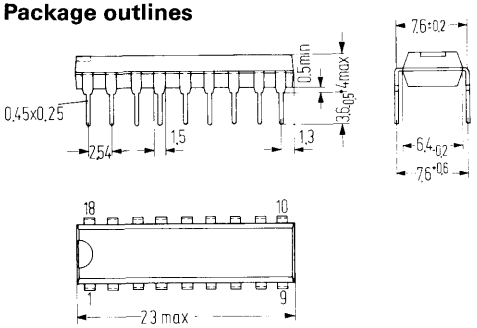
The MOS-circuit S 551, fabricated in the depletion-load-technology, constitutes in connection with the two bipolar circuits S 0280 (Station Decoder) and S 0281 (Message Decoder) and the MOS circuit S 552 (Area Decoder) the main portion of a traffic broadcast decoder used for car radios.

The traffic broadcast decoder (VRF-decoder) recognizes a VRF-station and the traffic messages (VDS) transmitted by it. An additional unit, the area decoder, makes it possible to identify the regional identity of a station. It is also possible with a VRF-decoder to search for a VRF-station automatically.

The S 551 has the task of recognizing the traffic broadcast message. A technical prerequisite for this is the presence of identification frequencies used by the various broadcasting stations in common:

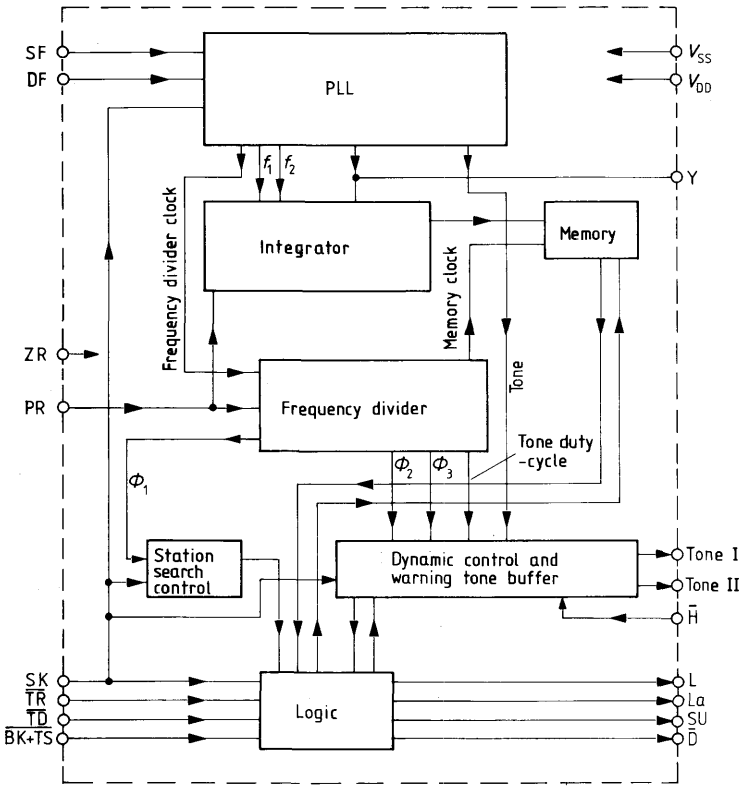
VRF-frequency: 57 kHz
VDS-frequency: 125 Hz

Package outlines



Plastic plug-in package
20 A 18 DIN 41866
(18 pins DIL)
Weight approx. 1.3 g

Block diagram



Pin connections

Pin No.	Designation
1	Transmission frequency SF
2	Message frequency DF
3	Loud-circuit LA
4	Message $\overline{D}$
5	Lamp L
6	Key radio $\overline{TR}$
7	Key message $\overline{TD}$
8	Area identification ($\overline{BK + TS}$)
9	Transmission identification SK
10	V_{SS}
11	Warning tone suppression $\overline{H}$
12	Station search SU
13	Tone II (undelayed)
14	V_{DD}
15	Tone I (delayed)
16	Y for testing purposes
17	Reset ZR
18	Test pin PR

Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	V_{SS}	−0.3	18	V
Input voltage	V_I	0	V_{SS} + 0.3	V
Power dissipation	P_{tot}		360	mW
Power dissipation per output (one output at a time)	P_Q		100	mW
Ambient operating temperature	T_{amb}	−25	+85	°C
Storage temperature	T_S	−40	+125	°C

All voltage values referred to V_{DD} = 0 V

Operating characteristics (all voltages referred to V_{DD} = 0 V)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_{SS}		9		16	V
Supply current	I_{SS}				15	mA
Inputs						
Transmission freq. SF (57 kHz) Message freq. DF (125 Hz)		Internal pull-high-resistor				
H-pulse width	t_{WH}	Duty cycle approx. 1:2				
L-pulse width	t_{WL}					
H-L transition time	t_{tHL}				3.5	µs
L-H transition time	t_{tLH}				3.5	µs
Harmless H-input current	$\lvert I_{IH} \rvert$				1	µA
L-input source resistance	R_{IQL}	to V_{DD}			10	kΩ
L-input source resistance	R_{IQL}	to V_{DD} + 1 V			6	kΩ
Key radio $\overline{TR}$						
Input voltages (see fig. 1)						
Key message $\overline{TD}$ (see fig. 2) Transmission identification SK (from DK analog circuit)		internal pull-high-resistor				
Harmless H-input current	$\lvert I_{IH} \rvert$				1	µA
L-input source resistance	R_{IQL}	to V_{DD}			5	kΩ
L-input source resistance	R_{IQL}	to V_{DD} + 1 V			3	kΩ

Operating characteristics (all voltages referred to V_{DD} = 0 V)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Area identification $\overline{BK + TS}$						
Warning tone suppression H (see fig. 3)						
H-input voltage	V_{IH}		V_{SS} −1.5		V_{SS}	V
L-input voltage	V_{IL}				2	V
Required input current	$\|I_I\|$				10	µA
Reset input ZR (see fig. 4)						
H-input voltage	V_{IH}	Reset	V_{SS} −1.3		V_{SS}	V
L-input voltage	V_{IL}	Release			2	V
H-pulse width	t_{WH}		20			µs
Required input current	$\|I_I\|$				10	µA
Outputs						
Station searching SU Loud-circuit La						
H-output voltage	V_{QH}	at /I/ = 0.05 mA	V_{SS} −5 V		V_{SS}	V
L-output voltage	V_{QL}	at /I/ = 1 µA			0.35	V
Short circuit current	$\|I_{Qmax.}\|$				10	mA
Lamp L						
H-output voltage	V_{QH}	at /I/ = 0.5 mA	V_{SS} −7 V		V_{SS}	V
L-output voltage	V_{QL}	at /I/ = 1 µA			0.35	V
Short circuit current	$\|I_{Qmax.}\|$				10	mA
Message $\overline{D}$						
H-output voltage	V_{QH}	at /I/ = 0.2 mA	V_{SS} −3 V		V_{SS}	V
L-output voltage	V_{QL}	at /I/ = 1 µA			0.35	V
Short circuit current	$\|I_{Qmax.}\|$				10	mA

Operating characteristics (all voltages referred to V_{DD} = 0 V)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Tone I (see fig. 5)						
H-output voltage (loud)	V_{QHl}	see test circuit No. 1	$\frac{6}{10} V_{SS}$	$\frac{9}{10} V_{SS}$	V_{SS}	V
L-output voltage	V_{QL}	see test circuit No. 1			100	mV
H-output voltage (medium)	V_{QHm}	see test circuit No. 1		$\frac{3}{10} V_{SS}$		V
H-output voltage (soft)	V_{QHs}			$\frac{1}{10} V_{SS}$		V
Turn-off damping	a	reference: operating level	60	80		dB
Sequence frequency	$\frac{1}{T}$			approx. 2		Hz
Tone frequeny	f_{tone}			approx. 1.7		kHz
Duty cycle	t_1/T			approx. 1/4		
Tone II (see fig. 6)						
H-output voltage	V_{QH}	see test circuit No. 2	$\frac{1}{2} V_{SS}$	$\frac{3}{4} V_{SS}$	V_{SS}	V
L-output voltage	V_{QL}	see test circuit No. 2			100	mV
H-output voltage (soft)	V_{QHs}	see test circuit No. 2		$\frac{1}{4} V_{SS}$		V
Turn-off damping	a	reference: operating level	60	80		dB
Sequence frequency	$\frac{1}{T}$			approx. 2		Hz
Tone frequency	f_{tone}			approx. 1.7		kHz
Duty cycle	t_1/T			approx. 1/4		

For operation with key "reset of function", by reapplication of supply voltage

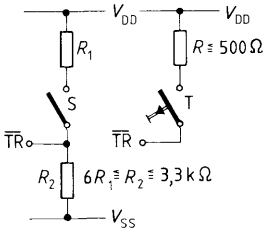


Figure 1

Connection of the $\overline{TD}$-input

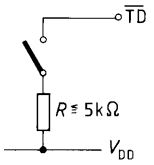


Figure 2

Suggestion for connection of the H-Input

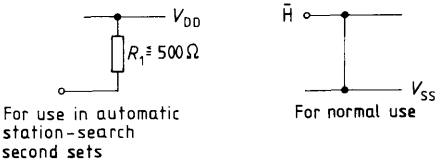


Figure 3

Circuit for automatic reset upon turn-on

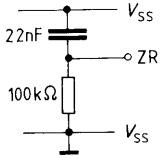


Figure 4

Output signals of the tone I output

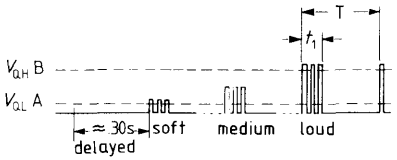


Figure 5

Output signals of the tone II output

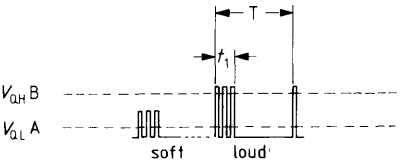
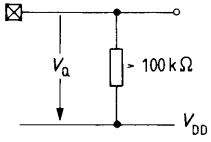
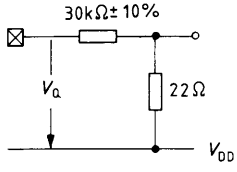


Figure 6

Test circuit 1
tone I



Test circuit 2
tone II



Testing of the turn-off damping
1. The supply voltage is kept constant during the measurement.
2. The measurement is taken with respect to the V_{DD}-pin.
3. The measurement is taken selectively for the basic frequency.

Functional description of the S 551

The S 551 contains 7 function blocks. The 4 blocks used for the recognition of the 125 Hz VDS tone constitute the largest portion of the circuit. They comprise a PLL-circuit (phase locked loop), an integrator, a memory and a frequency divider. The PLL-circuit is a 2-stage synchronous counter, the first portion of which can be switched between 28 and 29 counting steps. The subsequent divider has a 3-bit and a 4-bit output. As the clock frequency for the block, a 57 kHz rectangular signal is used. The two portions of the counter are connected in such a way that a 125 Hz signal appears at the 4-bit output as mean value. An incoming DF is applied to an Exclusive-OR-gate together with this signal; the output of this gate causes the switching of the counting steps of the first PLL-divider stage. The frequency at the 4-bit output is thereby displaced in time, until a stable divider ratio is produced at the output of the Exclusive-OR-gate. However, this is only possible when the DF amounts to approximately 125 Hz.

As an indicator whether the PLL has recognized a DF as correct, the output of a second Exclusive-OR-gate (Y) is used which has, as its input signals, the DF and also a reference frequency from the PLL divider for comparison, which has been phase-shifted by 90°. The output Y is consistently at an H-potential as long as the DF is proper. Small deviations of the DF with respect to the reference frequency are indicated by "low"-times within a Y-period. In the case of major frequency deviations, the PLL is continuously trying to fit the reference frequency to the DF, which results in a Y-signal appearing to be irregular as a first impression.

For the evaluation of the Y-signal, the integrator is used. It is an 11-bit synchronous up-down counter, which is defined in its counting direction by "Y". As clock frequencies, two clocks derived from the PLL-circuit are available (f_1 = 57 kHz 2^{-2} and f_2 = 57 kHz 2^{-3}). These clock signals are also selected by the Y-signal. The integrator is constructed in such a way, that due to Y = high – for upcounting slowly – and Y = low – for downcounting fast – the two possible counting combinations are achieved. For this reason a full-counting of the integrator is only possible when the L-portion within a Y-period is smaller than 1/3. An evaluation of the counter contents is done through a hysteresis circuit, with thresholds at the counter contents 1/4 full and 3/4 full. In order to make the DK less sensitive to short-time turn-offs of the VRF-broadcasting frequencies, the integrator is followed by a memory. The memory is a 4-bit synchronous up-down counter. Its clock frequency is about 57 kHz 2^{-14} and is derived from a central frequency divider. The counting direction of the memory is defined by a hysteresis circuit. When the hysteresis circuit indicates a full integrator, the memory will still be empty, but its output "DK" (internal signal) already indicates a message. From this point on, the counter counts up until it is full and remains that way. At this counting position, the memory is able to compensate for a gap in the VDS-frequency of approximately 4,6 s. After this time the memory is empty and the DK-signal goes high. A 9-bit counter serves as a central frequency divider. It has been constructed for the first 5-bit as a synchronous counter and for the rest as an asynchronous counter. The various input clocks used in the IC are taken from the appropriate divider stages or are decoded. As input clock the reference frequency of 125 Hz from the PLL is used.

An additional block consists of logic circuits which are not directly related to each other. The purpose of this circuit is an improvement in the comfort of handling.

The inputs $\overline{TR}$, $\overline{TD}$, $\overline{BK} + \overline{TS}$, SK and $\overline{H}$ and the internal signal DK determine the output functions L (lamp), La (loudcircuit), $\overline{D}$ (message decoding) SU (station searching).

A low level at input $\overline{TR}$ (key broadcast) indicates that no VRF-operation is intended. The input behaves in a bistable way; for switching it requires a low resistance driving. When the supply voltage is turned on again, the input is automatically set to VRF-operation.

A low level at input $\overline{TD}$ (key message) indicates that only road traffic information messages are to be reproduced.

A low level at input ($\overline{BK + TS}$) (area identification or key "only broadcast recognition") indicates that either the area identification circuit (BK-IC) has recognized the wanted area identification signal or that area distinguishing is not wanted.

A high level from the SK analog-IC at input SK (transmission identification) indicates that the station received is a VRF-station.

Through a low level at input $\overline{H}$, the circuit can be reprogrammed for the use in a station-searching second set. This function acts upon the warning tone.

The lamp output L shows a high level when the wanted kind of operation may be performed. For this purpose the SK (transmission identification)-input must receive an H-signal which means that a station with the proper transmission identification is being received. In addition, the ($\overline{BK + TS}$) (area identification or transmission identification only)-input must receive an L-signal which means that a station of the wanted area is being received or that no area identification is wanted.

This is also true in the case that no VRF function is wanted (key "broadcast" pushed: $\overline{TR} = 0$).

$L = SK\ (\overline{BK + TS})$

Output La from the loud-switch controls the loudspeaker amplifier. With a high level it sets the loudness to:

$La = D + TR + L \cdot \overline{TD}$

The message-identification output $\overline{D}$ indicates with a low level that a message is being recognized and the station received is located in the wanted area. With the key "broadcast" this signal is suppressed.

$D = DK \cdot L \cdot \overline{TR}$

Station-search output SU controls the automatic VRF-station searching motion.
(High level: search, low level: stop).

$\overline{SU}$ = TR + L + stop-pulse (SK)

The stop-pulse lasts about 0.5 s; it is produced every time a VRF-station has been found (SK = high) to give the BK-IC a chance to check whether or not the area identification is correct. (Own 4-bit asynchronous counter with frequency 57 kHz 2^{-12}). Station search is started with a delay to avoid response to brief noise signals received.

The output tone 1 produces a warning when no VRF-station is received from the wanted area.

Tone 1 = $\overline{\overline{TR} + L}$

However, the tone is turned-on no sooner than about 30 s after this condition has been established. Through a dynamic-stage it is produced at first four times soft then four times medium and finally loud.
(The delay and the dynamic control consists of a 5-bit asynchronous counter with a clock frequency of approx. 57 kHz 2^{-17}).

The output tone II is different from tone I by producing a warning tone undelayed and only in two dynamic-stages (four times soft and then loud). For this function a resistor to V_{DD} is required.

In connection with station-search second sets a warning tone will make no sense if no VRF-station can be received at all (poorly covered area). In this case the station search second set is to continue searching to discover a VRF-station as soon as possible. Not before a VRF-station has been found, which does not belong to the wanted area, however, a warning tone will make sense again indicating the possibility of an improved operation.

Operation:

If no VRF-station can be received, the SU-signal remains low. As soon as a VRF-station has been found during the periodic searches, periodic pulses with SU = high occur. When the $\overline{H}$-input is low, the warning tone is blocked if SU remains low for a period exceeding 20 s.

Note:

Inputs PR and Y are intended for testing. They must not be externally connected for other purposes.

Area Decoder for FM Road Traffic Information Service

S 552

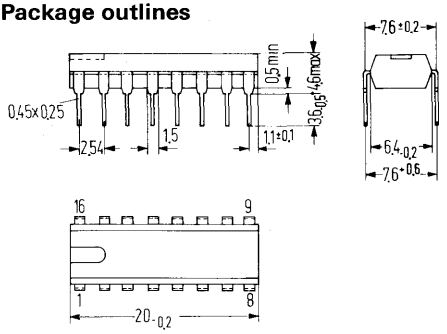
Preliminary data

Type	Ordering code
S 552	Q 67100–Z 110

The MOS circuit S 552, fabricated in the depletion-load technology is an extension of the two bipolar circuits S 0280 (transmission decoder), S 0281 (message decoder) and the MOS-circuit S 551 (message decoder), which together constitute the main portion of a traffic broadcast decoder used in car radios.

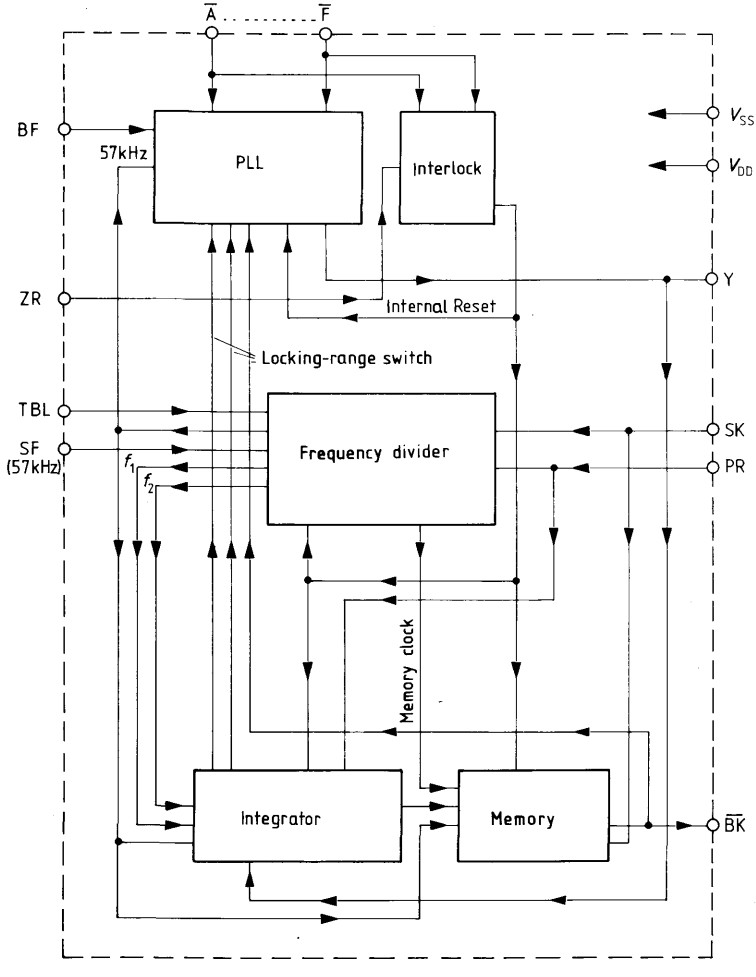
The S 552 recognizes the identification frequency of a VRF-station of a specific region and switches traffic messages of only this station to the loudspeaker. The S 552 has been designed for 6 different area frequencies, which can be pre-selected at inputs $\overline{A}$ to $\overline{F}$.

Package outlines



Plastic plug-in package
20 A 16 Din 41866
(16 pins DIL)
Weight approx. 1,2 g

Block diagram



Pin connections

Pin No.	Designation
1	Area frequency BF
2	Transmission identification SK
3	Reset ZR
4	Testing PR } for testing purposes
5	Y-input/output } for testing purposes
6	Clock blocking TBL } for testing purposes
7	Station frequency SF
8	V_{SS}
9	V_{DD}
10	Area selection $\overline{F}$
11	Area selection $\overline{E}$
12	Area selection $\overline{D}$
13	Area selection $\overline{C}$
14	Area selection $\overline{B}$
15	Area selection $\overline{A}$
16	Area identification $\overline{BK}$

Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	V_{SS}	−0.3	18	V
Input voltage	V_I	0	V_{SS} + 0.3	V
Power dissipation	P_{tot}		400	mW
Power dissipation per output	P_Q		100	mW
Ambient operating temperature	T_{amb}	−25	+85	°C
Storage temperature	T_S	−40	+125	°C

All voltages referred to V_{DD} = 0 V

Operating characteristics (all voltages referred to V_{DD} = 0 V)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_{SS}		9		16	V
Supply current	I_{SS}				15	mA
Inputs						
Transmission frequency SF (57 kHz)		internal pull-high resistor				
Area frequency BF (A = 23.79 Hz, B = 28.32 Hz C = 34.98 Hz, D = 39.65 Hz, E = 45.75 Hz, F = 54.04 Hz)						
H-pulse width	t_{WH}	duty cycle approx. 1:2				
L-pulse width	t_{WL}					
H-L transition time	t_{THL}					
L-H transition time	t_{TLH}				3.5	µs
Harmless					3.5	µs
H-input current	I_{IH}				1	µA
L-input source resistance	R_{IQL}	to V_{DD}				kΩ
L-input source resistance	R_{IQL}	to V_{DD} + 1 V				kΩ
Transmission identification SK (from DK-analog circuit)		internal pull-high resistor				
Harmless H-input current	$\lvert I_{IH} \rvert$				1	µA
L-input source resistance	R_{IQL}	to V_{DD}			5	kΩ
L-input source resistance	R_{IQL}	to V_{DD} + 1 V			3	kΩ

Operating characteristics (all voltages referred to V_{DD} = 0 V)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Programming inputs $\overline{A}$ . . . $\overline{F}$ (see fig. 1)		internal pull-high resistor				
Harmless H-input current	$\lvert I_{IH}\rvert$				1	µA
L-input source resistance	R_{IQL}	to V_{DD}			5	kΩ
L-input source resistance	R_{IQL}	to V_{DD}+1V			3	kΩ
Reset input ZR (see fig. 2)						
H-input voltage	V_{IH}	reset	V_{SS}–1.3V		V_{SS}	
L-input voltage	V_{IL}	released			2	V
H-pulse width	t_{WH}		20			µs
Required input current	I_I				10	µA
Area identification $\overline{BK}$						
H-output voltage	V_{OH}	at /I/ <10 µA	V_{SS}–1.3V		V_{SS}	
L-output voltage	V_{OL}	at /I/ <10 µA			1.5	V
Short circuit current	$I_{Qmax.}$	continuous short circuit proof			1	mA

Connection of programming inputs $\overline{A}$ . . . $\overline{F}$

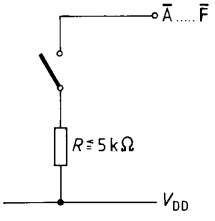


Figure 1

Circuit for automatic reset upon turn-on

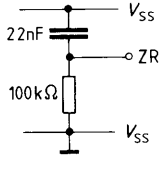


Figure 2

Functional description of the S 552

The area decoder circuit S 552 is an extension of the VRF-decoder-system. It is used to recognize the area frequency (identification frequency of the VRF-station of a region). The S 552 has been designed for 6 different area frequencies (BF), which are preselected by means of an L-level at the programming inputs $\overline{A}$-$\overline{F}$. This can be done with a switch, which briefly opens all inputs when turned, as well as with a switch which bridges several inputs simultaneously when operated.

The circuit contains a PLL-portion like the S 551. It consists of three synchronous counters in series. The first of these counters can be switched between the two counting positions 23 and 25. In addition, for an extension of the locking range, two additional counter combinations are possible: 21/27 and 19/29. The switching of the locking range is done by an integrator following the PLL. The second divider of the PLL-circuit can be switched externally through the $\overline{A}$-$\overline{F}$-inputs. With an L-level at $\overline{A}$ it divides by 25, at $\overline{B}$ by 21, at $\overline{C}$ by 17, at $\overline{D}$ by 15, at $\overline{E}$ by 13 and at F by 11. In order to convert, through division, a 57 kHz SF-signal into a BF-signal, the PLL contains an additional 2-bit divider. Corresponding to the programming inputs $\overline{A}$ . . . $\overline{F}$ used, the PLL generates an internal BF-signal. An externally applied BF (at the BF-input) is applied to an exclusive-OR-gate together with the internal signal. The output of this gate causes switching of the counting steps at the first divider stage (e.g. 23/25). Thereby the internal BF is shifted in phase until a stable switching ratio has been obtained.

As an indication, that the PLL has recognized a BF properly, the output of a second exclusive-OR (Y-signal)-gate is used; the inputs of this gate are the internal reference frequency, shifted by 90°, and the BF.

In case of a stable switching ratio mentioned above, Y has a high level and thereby indicates the recognition of a proper BF. If the BF received is wrong, the Y-output shows an irregular signal.

Just as in the case with S 551, the S 552 also contains an integrator and a memory. Both blocks receive their clock frequency from an internal frequency divider. This frequency divider consists essentially of a synchronous counter, which generates the integrator clock, and an asynchronous divider operated in series, which supplies the memory clock.

The integrator is an 8-bit synchronous up-down counter. Its clock frequency depends on the PLL output. For Y = high it amounts to approx. 2370 Hz and at Y = low 4750 Hz. In addition, the direction of counting of the integrator is determined by the level of the Y-signal. At the high clock frequency it counts down (at Y = low) and at the low frequency it counts up (Y = high). The minimum duty cycle of the Y-signal for upcounting of the integrator is <1:3 for Y = low.

An evaluation of the contents of the counter is done by means of a hysteresis-circuit with thresholds at counter contents 1/4 full and 3/4 full. In addition, the integrator stages with the highest significance determine a change of the locking range in the first PLL-divider stage.

When the integrator is empty (0 to 1/4), the PLL-divider can be switched between 19 and 29 counting steps, when the integrator has been partially filled (1/4 to 1/2) between 21 and 27 steps and if it is filled more than 1/2 or if $\overline{BK}$ = low between 23 and 25 counting steps.

When the integrator is full or when the memory is not entirely empty, the output $\overline{BK}$ = low. The memory will bridge a brief disappearance of SK or BF. It consists of a 4-bit synchronous up/down counter and the maximum storage time amounts to approx. 6s. Its clock frequency is approx. 2.3 Hz. When the hysteresis output shows a full integrator the memory counts up and for an empty integrator down. The hysteresis signal, together with the Q_1-outputs of the individual memory bits, forms the $\overline{BK}$-signal through a gate. Therefore the $\overline{BK}$-output remains low for additional 6s after the integrator has counted down to zero.

Note:

The inputs TBL, PR and Y are intended for testing purposes. They must not be connected externally.

Preliminary data

Type	Ordering code
TDA 1195	Q 67100–J 389

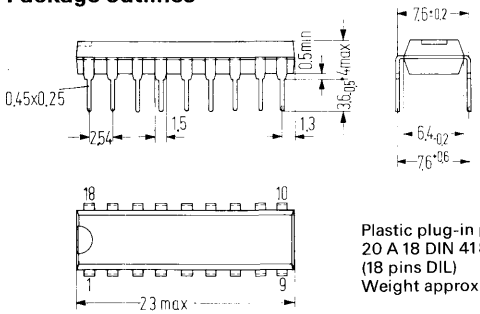
The circuit TDA 1195 contains four electronic switches. There are two common control inputs for each set of two switches. The control inputs U_{AB} and U_{CD} are intended for the switching, K_{AB} and K_{CD} are chip-select inputs. The TDA 1195 is an MOS circuit in p-channel depletion technology and therefore shows bidirectional switching properties (i.e. inputs and outputs are freely selectable, because a signal can flow in both directions).

The main application area of the TDA 1195 is the switching of signal sources in the entertainment area, e.g. in AF-amplifiers and radio- and taperecorder-sets. A further application area is the use as a measuring-input switch in the instrumentation and control field.

Advantages of the TDA 1195.

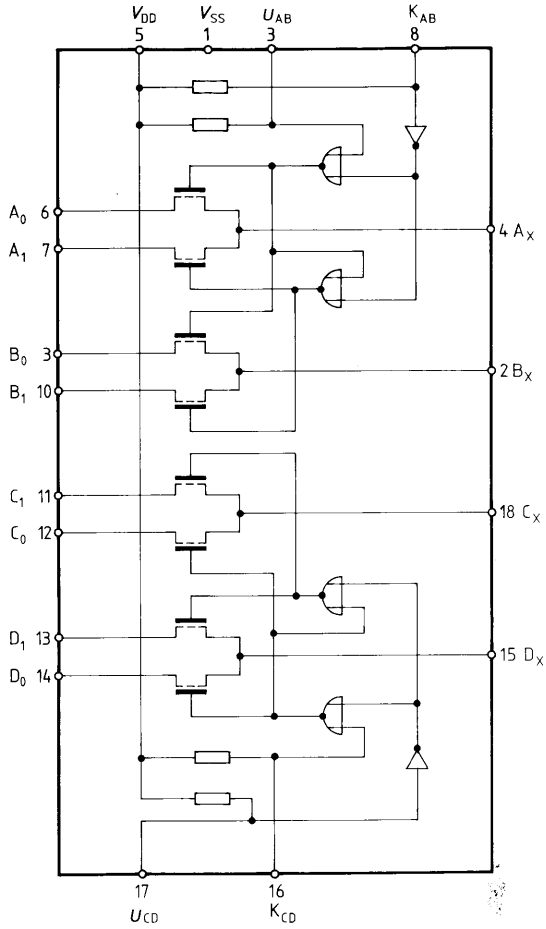
- Reduction of the AF cable length to a minimum, as the TDA 1195 can be installed right at the place where switching is required.
- Replacement of the (mostly shielded) AF-cables connecting the location of switching with the control switch at the front plate with a simple control lead.
- The control inputs are at an L-potential when not connected. Therefore normally open or normally closed contacts can be used for control.
- High noise radiation resistance, as no diodes are used in the switching line which could possibly demodulate a strong RF-radiation received.
- High cross-talk damping between the signal inputs and outputs.
- High level of modulation, max. 6 V_{eff}.
- Low harmonic distortion level, typ. 0.05%. In medium-class HiFi-equipment no additional external circuitry is required. For HiFi-equipment of the high class, one emitter-follower each at the signal inputs is sufficient to achieve a harmonic distortion factor of <0,02% (at 5 V_{eff}, kHz).

Package outlines

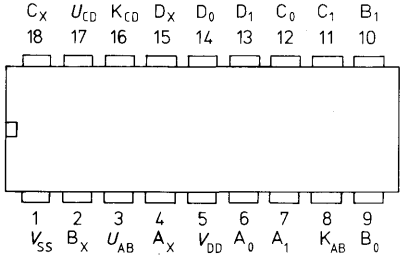


Plastic plug-in package
20 A 18 DIN 41866
(18 pins DIL)
Weight approx. 1,3 g)

Simplified FET-diagram



Pin connections, top view



Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	−21	0.3	V
Input voltage	V_I	−21	0.3	V
Ambient operating temperature	T_{amb}	0	+70	°C
Storage temperature	T_S	−55	+125	°C

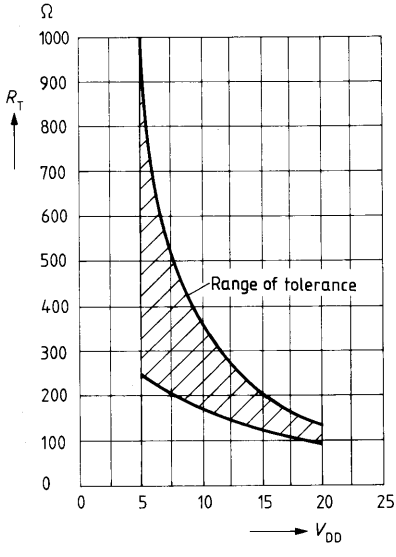
Operating characteristics (all voltages referred to V_{SS} = 0 V)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_{DD}		−21		−5	V
Supply current	I_{DD}		−0.8	−0.3		mA
Control inputs (U- and K inputs)						
H-Input voltage	V_{IH}		−0.8		0.3	V
L-input voltage	V_{IL}	externally controlled	−21		−4	V
L-input voltage	V_{ILO}	input open, see test circuit 1	V_{DD}		V_{DD} + 2	V
H-input current	I_{IH}	short circuit to V_{SS}	−20		−4	µA
HL-transition time	t_{THL}				100	µs
LH-transition time	t_{TLH}				100	µs
H-pulse width	t_{WH}		100			µs
Input capacitance	C_I				10	pF

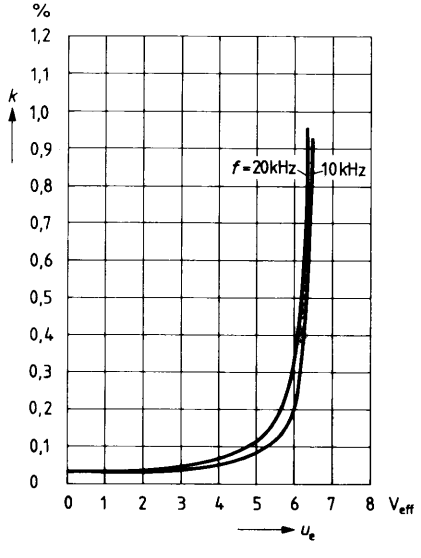
Operating characteristics (all voltages referred to V_{SS} = 0 V)

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Bidirectional signal inputs or outputs (A-, B-, C-, and D-inputs)						
H-input voltage	V_{IH}				0.3	V
L-input voltage	V_{IL}	externally controlled	V_{DD} + 3			V
Switch resistance	R_T	V_{DD} = −20 V			150	Ω
Operating point		see test circuit 2		$V_{DD}/2$		V
Harmonic distortion	k	see test circuit 3 at V_{eff} = 5 V, 20 kHz, V_{DD} = −21 V			0.02	%

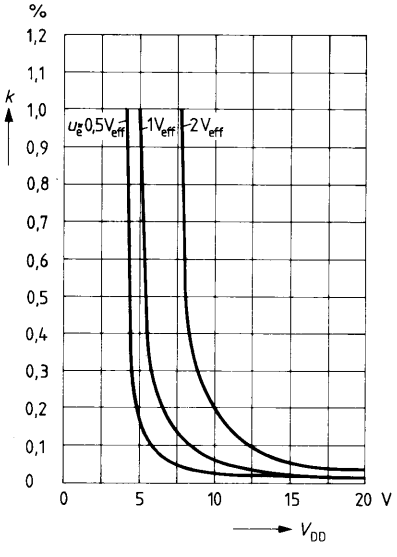
Switch resistance R_T
as a function of the supply voltage V_{DD}



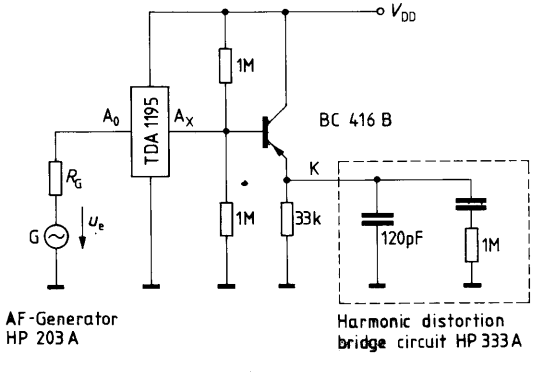
Increase of harmonic distortion as a function of the voltage u_e switched
(V_{DD} = 20 V, R_G = 600 Ω)
Parameter is the frequency f



Harmonic distortion as a function of the supply voltage V_{DD}
(f = 10 kHz, R_G = 47 kΩ)
Parameter is the switched voltage u_e



Test circuit for harmonic distortion

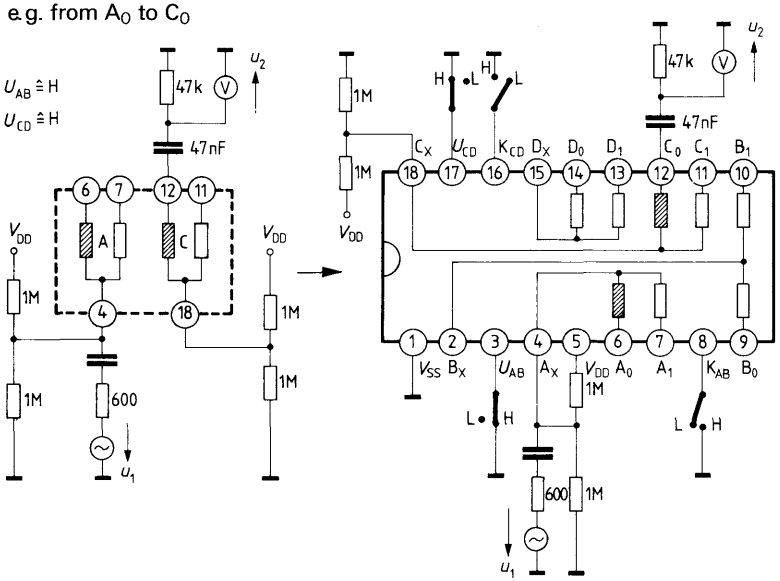


The harmonic distortion can be considerably improved by using a pre-emitter-follower-stage according to test circuit 3 with circuit TDA 1195.

Crosstalk-values (measured data) in dB at 10 kHz, R_G = 47 kΩ
(V_{DD} = −21 V, u_1 = 5 V_{eff})

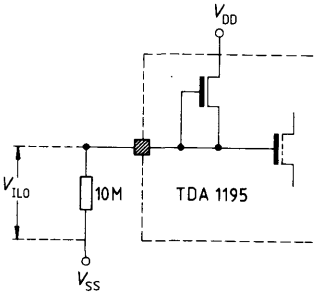
Pin		6	7	9	10	11	12	13	14
	Switch-designation	A_0	A_1	B_0	B_1	C_1	C_0	D_1	D_0
6	A_0	0	52	62	81	78	77	74	74
7	A_1	51	0	65	64	76	76	75	75
9	B_0	62	65	0	63	67	70	77	76
10	B_1	77	65	62	0	51	62	72	73
11	C_1	78	77	63	51	0	50	60	70
12	C_0	78	77	71	62	50	0	53	60
13	D_1	75	75	78	71	59	52	0	48
14	D_0	75	76	79	73	71	59	52	0

Test circuit for crosstalk
e.g. from A_0 to C_0



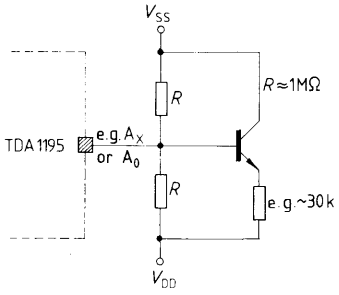
The values of crosstalk measured are strongly affected by the construction of the test circuit. Through an appropriate layout of the PC-board, the crosstalk values can further be improved considerably.

Test circuits



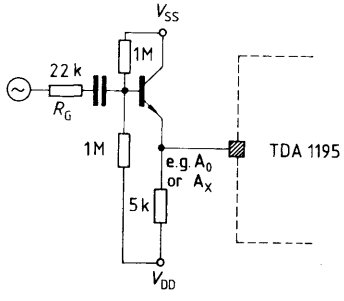
▨ = Connection of a control input

Test circuit 1



▨ = Connection of a signal output
V_{DD} = Equipment common

Test circuit 2

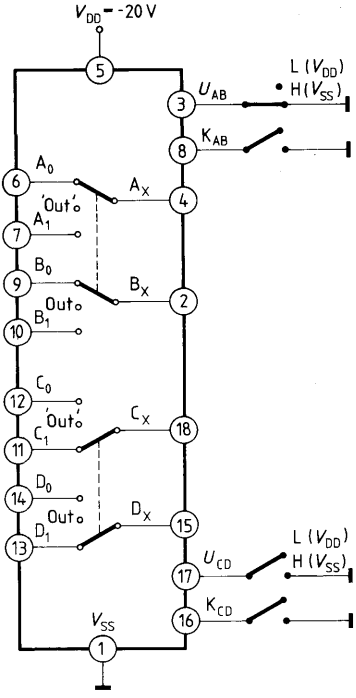


V_{DD} = Equipment common ⟶ npn.-trans.
V_{SS} = Equipment common ⟶ pnp.-trans.

Note: If operating point $V_{DD}/2$ is fixed at the AF-input, the AF-output may be operated without connection of a resistor

Test circuit 3

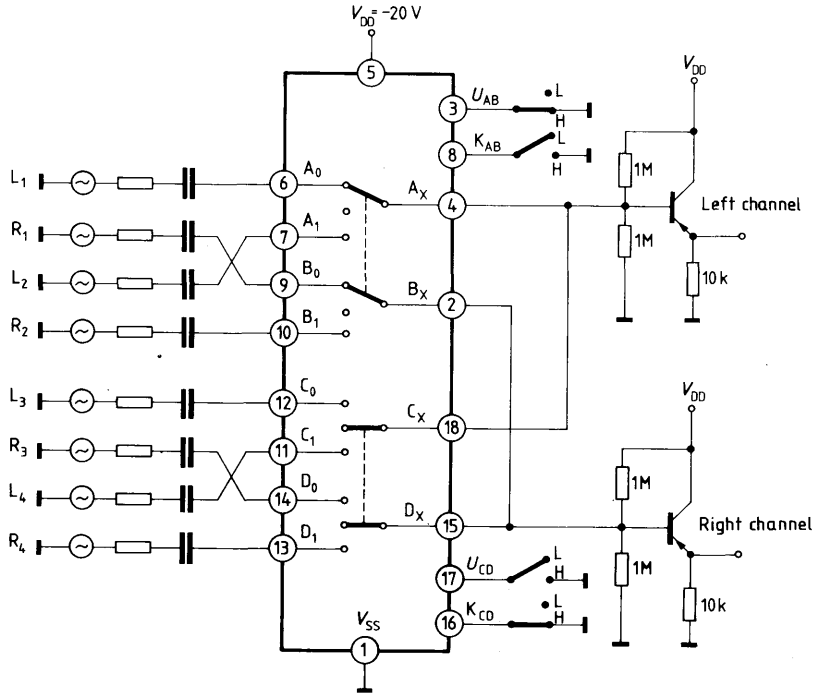
Switching functions of the TDA 1195 in principle



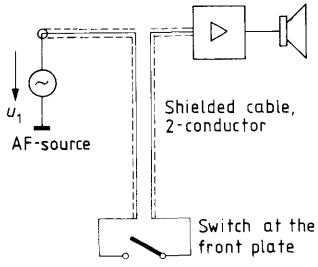
control line		switch	
K_{AB}	U_{AB}	A	B
H	H	'Out'	'Out'
H	L	'Out'	'Out'
L	H	A_0-A_X	B_0-B_X
L	L	A_1-A_X	B_1-B_X

control line		switch	
K_{CD}	U_{CD}	C	D
H	H	'Out'	'Out'
H	L	'Out'	'Out'
L	H	C_0-C_X	D_0-D_X
L	L	C_1-C_X	D_1-D_X

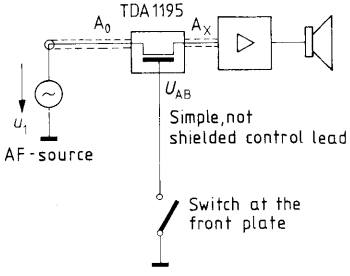
Switching of 4 AF stereo sources to one stereo amplifier, using the TDA 1195



Elimination of long, shielded cables when switching AF signal sources



Conventional switching of an AF-source to an amplifier



Simplified switching with the AF-switch TDA 1195

MOS-Circuits for Consumer Applications

Preliminary data

Type	Ordering code
S 181-1	Q 67100–Z 59

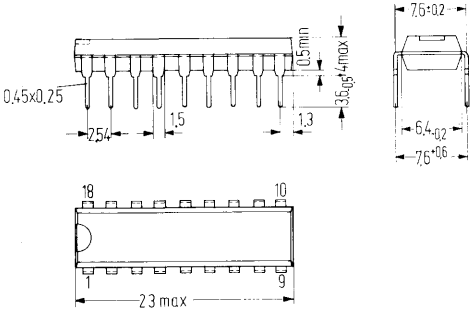
The S 181-1 is a highly integrated monolithic MOS-circuit in p-channel low voltage technology with depletion load transistors. It has been designed for the following functions:

Control of the aperture stepping-motor, with forward and reverse directions of rotation (4-phase steps)

Control of the film transport motor, with various adjustable timing programs.

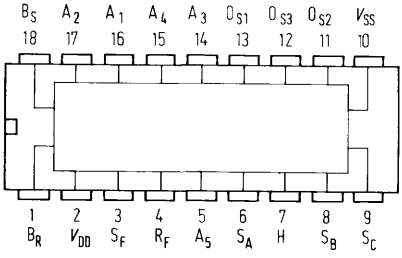
- Single frame function
- Automatic single-frame repetition;
  frame frequency externally continuosly adjustable from 0.1 to 60 seconds
- Automatic four-exposure title pictures
- 5 seconds run following a delay of 10 seconds
- 10 seconds run following a delay of 10 seconds

Package outlines



Plastic plug-in package
20 A 18 DIN 41866
(18 pins DIL)
Weight approx. 1,3 g

Pin connections, top view



Inputs:

Inputs for aperture control:

B_S aperture stepping motor start-stop
B_R aperture stepping motor direction

S_A, S_B, S_C } coding inputs for timing programs

S_F switching input for initiating the timing program (film transport)

O_{S1}, O_{S2}, O_{S3} } inputs for the connection of oscillator components

H testing input (usable for external frequency application to O_{S1}, O_{S2}, O_{S3})

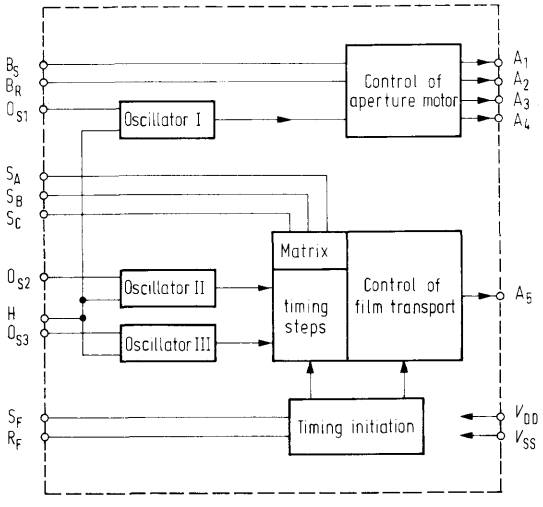
V_{DD}, V_{SS} } supply voltages

Outputs:

A_1, A_2, A_3, A_4 } outputs for the control of the aperture stepping motor

A_5 output for the control of the film transport motor

Block diagram



Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage, Voltage at all pins	referred to V_{SS} = 0 V	V_{DD} V	−25 −25	0.3 0.3	V V
Storage temperature		T_S	−55	+125	°C
Ambient operating temperature		T_{amb}	−20	+50	°C

Operating characteristics (T_{amb} = 25°C)

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	V_{SS} = 0 V	−4.8	−4.5	V
L-input voltage	V_{IL}	V_{DD} = −4.5 V		−4.2	V
H-input voltage	V_{IH}		−0.8		V
L-output voltage	V_{QL}			V_{DD} −0.3	V
H-output voltage	V_{QH}	$I_Q \leq 1$ mA	−1		V
Supply current	I	I_Q = 0 mA		3	mA
Oscillator frequency	f_{osz}			100	kHz

Logic functions:

1. Control of the aperture stepping motor with forward and reverse direction:

a) forward direction:

inputs		outputs			
B_S	B_R	A_1	A_2	A_3	A_4
H	L	H	L	L	H
H	L	H	L	H	L
H	L	L	H	H	L
H	L	L	H	L	H

b) reverse direction

inputs		outputs			
B_S	B_R	A_1	A_2	A_3	A_4
H	H	H	L	L	H
H	H	L	H	L	H
H	H	L	H	H	L
H	H	H	L	H	L

If $B_S \rightarrow$ L, then all outputs A_1, A_2, A_3, A_4 will also be L-independant of B_R.

2. Control of the film transport motor

a) coding inputs for the timing program and normal film transport:

Abbreviation	Function	Program switch setting** S_A	S_B	S_C
0	timing program turned off* (normal camera function)	L	L	L
E	single frame	L	L	H
5 sec	5 seconds running time	L	H	H
10 sec	10 seconds running time	H	H	H
T_I	title picture	H	H	L
E_A	single-frame repeat automatic	H	L	L

Notes:

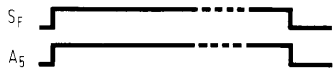
* Additional external switch connecting S_F and A_5 for normal film transport. Initiation of film transport through S_F.

** For switching into a new program position, the program switch must first pass through S_A, S_B, S_C = L, L, L, to cause reset, i.e. the contacts must briefly be opened.

b) Pulse diagrams for timing program and normal film transport

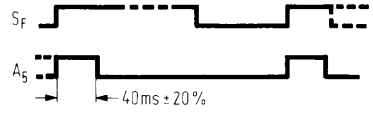
Normal camera function:

Position: "0"



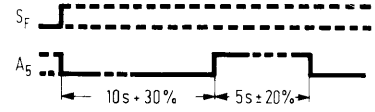
Single frame

Position: "E"



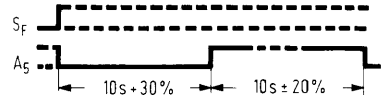
5 seconds run

Position: "5 sec."



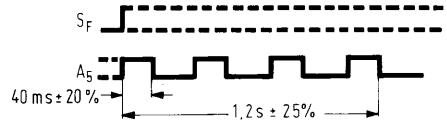
10 seconds run

Position: "10 sec."



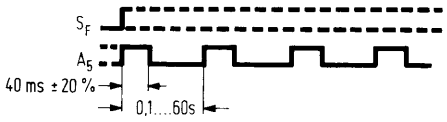
Automatic title picture sequence

Position: "T"



Automatic single-frame repetition

Position: "E_A"



c) Oscillator inputs for 3 internal oscillators

Input O_{S1}:

Through an external RC-circuit, the oscillator frequency is adjusted for the aperture stepping motor (in a range from approx. 10-100 Hz oscillator frequency). 4 tracks at typically 132 ms/track correspond to 7,5 Hz phase-steps.

Input O_{S2}:

Through an external RC-circuit, the oscillator frequency for pulse length and pulse dwells is adjusted for the timing programs E, 5 sec., 10 sec., T_I (200 Hz oscillator frequency).

Input O_{S3}:

Through an external RC-circuit, the oscillator frequency for the pulse dwells is adjusted for timing program E_A. (Oscillator frequency range approx. 150 Hz-100 kHz).

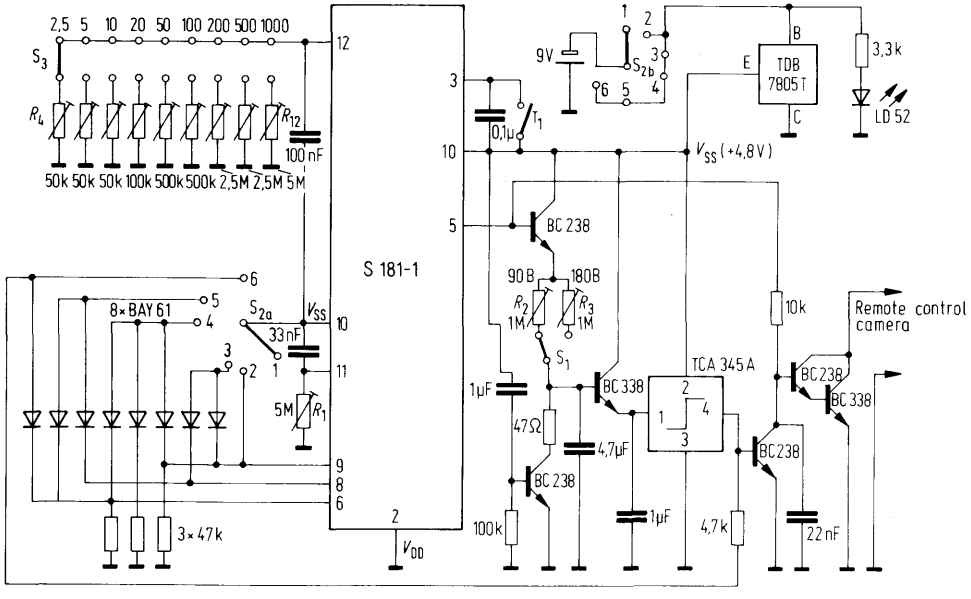
d) Testing input H:

When input H is at an H-potential, the oscillators operate as Schmitt-triggers.

When input H is not connected, the oscillators are free to run and input H is automatically at an L-potential.

When using this circuit, possibly existing patent rights of the AGFA Company must be taken into consideration.

Application circuit using the S 181-1
with fast-motion-picture circuit



Description

The application circuit covers the different timing programs contained in the S 181-1 (single frame, five seconds run, ten seconds run, title-picture automatic) and an additional function used to create fast-motion effects.

Selection of the timing programs

The selection of the programs is done using "S_2"; hereby the program chosen is initiated through key T_1.

S_2-switch in position: 1: Off
2: Single frame
3: Five seconds run (automatic exposure)
4: Ten seconds run (automatic exposure)
5: Automatic title-picture sequence
6: Fast motion

The functional sequences for positions 1 through 5 can be seen from the description of the S 181-1 control of the film transport motor.

Position 6 is realized in the following way:
The wanted fast-motion factor, between 2.5 and 1000, is available through an appropriate setting of switch S_3. The length of the individual scenes, 90 frames or 180 frames, is selected using switch S_1. The resulting range of variations possible can be obtained from the following table:

Table for fast-motion functions

Fast-motion factor	Frames per second	Time between frames	Running time for number of frames* 90 frames	180 frames
2.5	7.2	0.14 s	12.5"	25"
5	3.6	0.28 s	25"	50"
10	1.8	0.56 s	50"	1'40"
20	0.9	1.1 s	1'40"	3'20"
50	0.36	2.8 s	4'10"	8'20"
100	0.18	5.5 s	8'20"	16'40"
200	0.09	11 s	16'40"	33'20"
500	0.036	28 s	41'40"	1^{h}22'40"
1000	0.018	56 s	1^{h}23'20"	2^{h}46'40"

*) Corresponding to a picture-taking time of 5 or 10 seconds, respectively, in normal operation (18 frames per second).

The following instructions simplify the setting for fast-motion functions.

Setting-instructions

1. In position "fast motion", set pulse width of the output signal at pin 5 of the S 181-1 to approx. 40 ms using R_1 (5 MΩ).
2. Limit length of scene to 90 or 180 frames using R_2 and R_3.
3. Select the appropriate values of "time-between frames" shown in the above table, using R_4 through R_{12}.

Type	Ordering code
SAJ 205	Q 67100–J 398[1])

The circuit SAJ 205, fabricated in MOS-depletion-technology, is particularly suited for an application in electronic organs.

The SAJ 205 contains 8 divider stages and 8 digital/analog converters to form the staircase. At nine outputs, a wave of either rectangular pulses or staircase pulses (switchable) is produced at a repetition frequencies

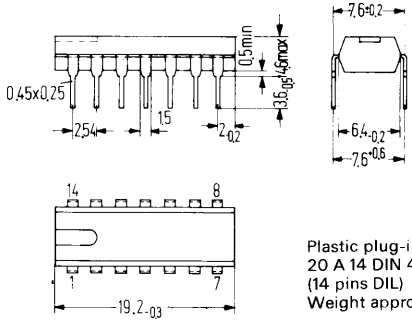
$f_1, \frac{f_1}{2}, \frac{f_1}{4}, \ldots \frac{f_1}{256}$.

The staircase voltage can be used to generate a frequency spectrum with even-number and odd-number harmonics. The nine outputs of the SAJ 205 permit the realization of a tone generator for nine octaves. Division of the input frequency is done exactly, using digital frequency divider stages.

Advantages

- Simple, economic and space-saving construction of the staircase generator.
- The exact synchronization of the divider stages is automatically produced through the digital frequency division, in contrast to conventional staircase generators (blocking oscillators).

Package outlines



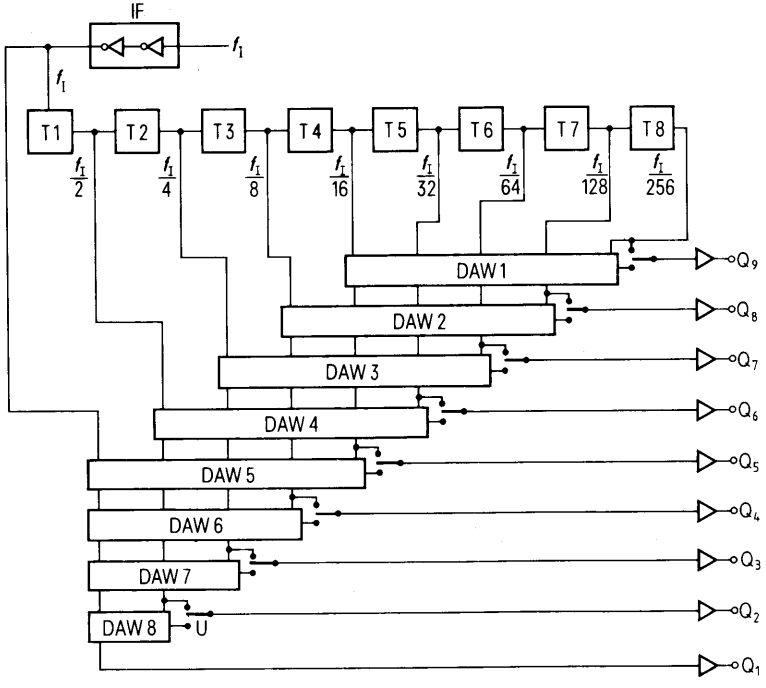
Plastic plug-in package
20 A 14 DIN 41866
(14 pins DIL)
Weight approx. 1.1 g

1) Our supply capacities for the SAJ 205 are limited. Please obtain information, before starting a development, from the Siemens Office serving your area.

Pin connections

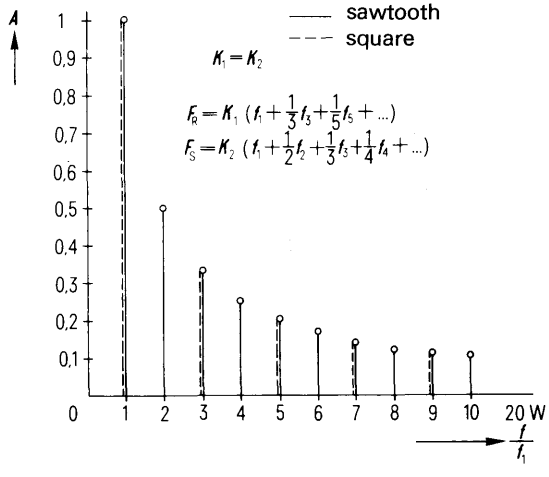
Pin-No.	Connection	Frequency
1	V_{DD}	
2	f_I	
3	mode	
4	V_{SS}	
5	V_{GG}	
6	output Q_1	f_I
7	output Q_2	$f_I/2$
8	output Q_3	$f_I/4$
9	output Q_4	$f_I/8$
10	output Q_5	$f_I/16$
11	output Q_6	$f_I/32$
12	output Q_7	$f_I/64$
13	output Q_8	$f_I/128$
14	output Q_9	$f_I/256$

Block diagram



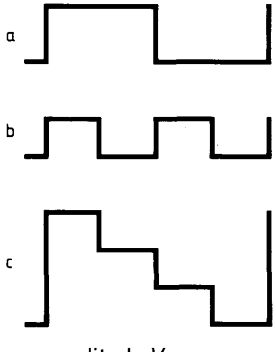
U Switch to change from square to saw tooth wave
IF Pulse shaping stage

Comparison of the frequency spectrums of sawtooth and square signals, for equal amplitudes of the fundamental wave



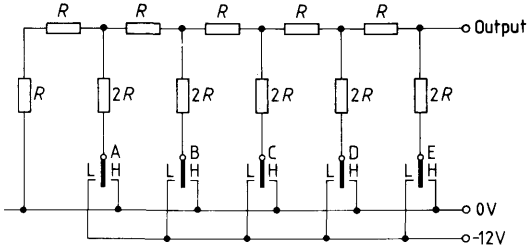
f_1 fundamental wave
f multiple of the fundamental wave
F_R frequency spectrum
F_S frequency spectrum sawtooth

Principle of generating the staircase

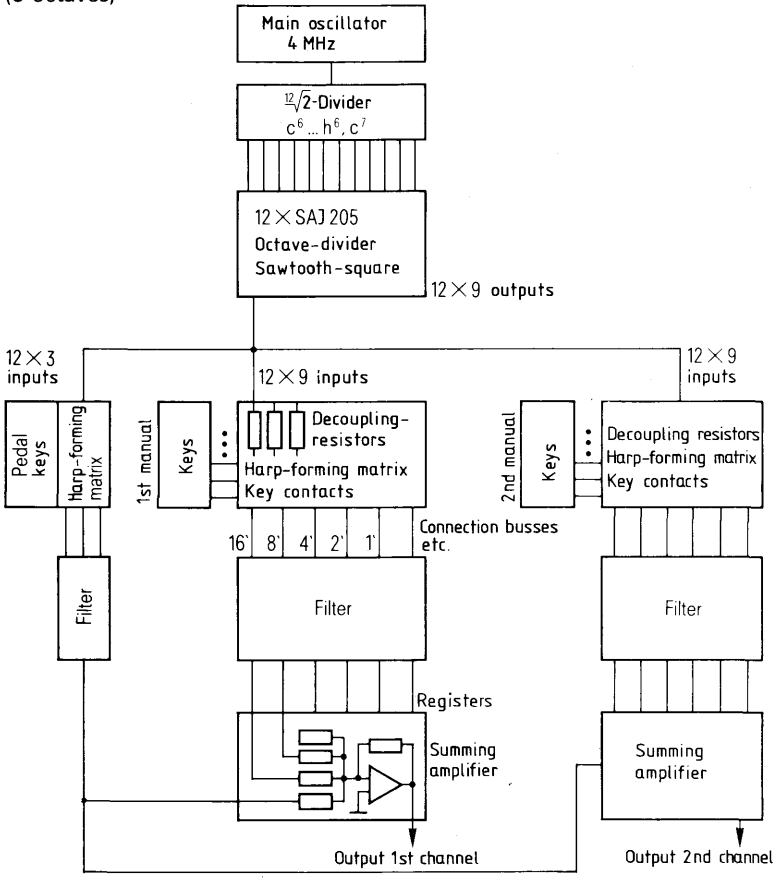


a amplitude V
b amplitude $\frac{V}{2}$
c summation in digital-analog-converter

Principle of the digital-analog converter in the SAJ 205



Block diagram of an electronic organ using 12 organ circuits SAJ 205
(9 octaves)



Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	−20	0.3	V
	V_{GG}	−22	0.3	V
Input voltage	V_I	−20	0.3	V
Ambient operating temperature	T_{amb}	0	+50	°C
Power dissipation	P_{tot}		450	mW
Storage temperature	T_S	−55	+125	°C

Static operating characteristics

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}		−13	−11	V
	V_{GG}		−22	−19	V
Supply current	I_{DD}	without load resistor	−2		mA
	I_{GG}	without load resistor	−15		mA
H-input voltage	V_{IH}		−1		V
L-input voltage	V_{IL}			−6	V
H-input voltage at mode-input	V_{MH}		−1		V
L-input voltage at mode-input	V_{ML}			−6	V
H-output voltage for square operation	V_{QHR}	without load resistor	−5.2	−2.8	V
L-output voltage for square operation	V_{QLR}	without load resistor	−15.7	−13.3	V
L-input resistance	R_{IL}			2	MΩ
Input capacitance	C_I			5	pF

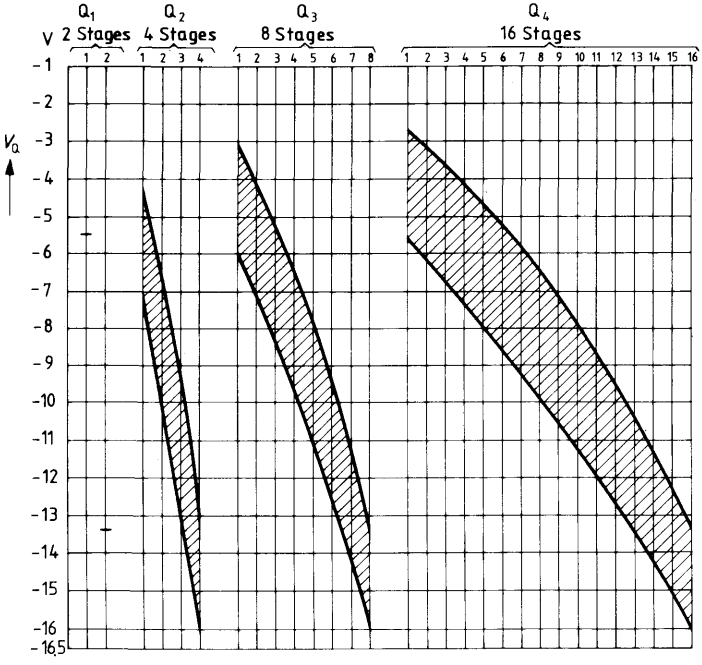
Output voltage for staircase voltage operation: See following table.

Dynamic operating characteristics

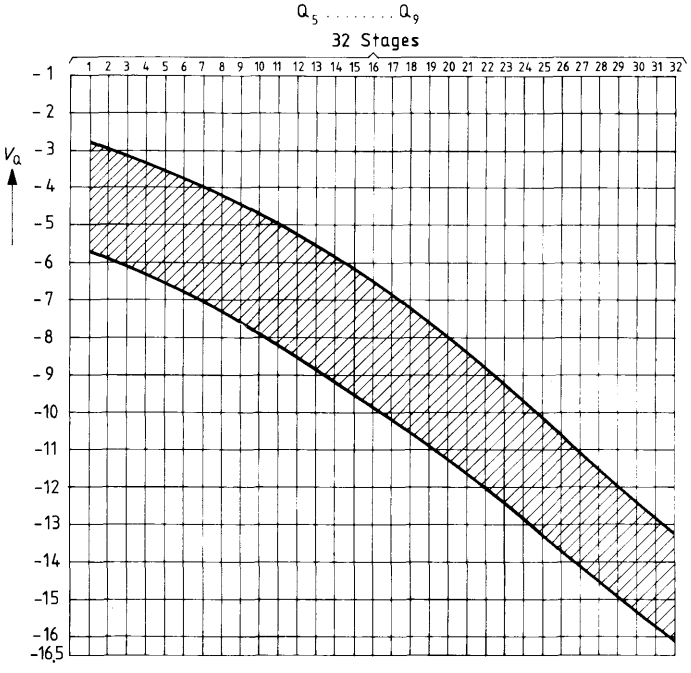
Information input (see fig. 4)					
Input frequency	f_I		0	50	kHz
HL-transition time	t_{THLI}			25	µs
LH-transition time	t_{TLHI}			25	µs

All voltages are referred to V_{SS} = 0 V

Output levels of the staircase voltages (range of tolerance)
$V_{DD} = -12$ V; $V_{GG} = -22$ V



Output levels of the staircase voltages (range of tolerance)
$V_{DD} = -12$ V; $V_{GG} = -22$ V



Instructions for the square pulse operation

An L-level must be applied to the mode-input.

Duty cycle

The duty cycle at output Q_1 is defined by the shape of the input signal. The duty cycle of all other outputs is 1:1.

Counter operation

The output signals (2-9) change with the negative edge of the input signal. Resetting of the divider stages is possible using an H->L-rise of the V_{DD} voltage.

The voltage rise time should not be shorter than 20 µs. After the reset, the outputs resume an H-level.

Instructions for the staircase voltage operation

An H-level must be applied to the mode-input.

Duty cycle

The duty cycle at output Q_1 is determined by the shape of the input signal.

The input signal is used for the staircase generation. To yield a uniform staircase, the duty cycle of the input signal should be approx. 1:1.

After resetting the divider stages (during the V_{DD}-rise time) the outputs assume an L-level during the staircase voltage operation.

General notes

1. V_{DD} determines the alternating voltage amplitude.
   To avoid amplitude fluctuations, V_{DD} should therefore be stabilized.
   To avoid major non-linearities in the shape of the staircase voltage, V_{DD} should be selected to be not higher than $|-13\ V|$.

2. $V_{GG} = |-22\ V|$ must not be exceeded in any case as long as proper functioning must be ensured.

3. The outputs contain a source-follower-stage with a built-in constant-current load of approx. 1 mA to V_{SS}. External pre-loading resistors are not required. The fluctuations of the output voltage due to fluctuations of the output load from $R_L = \infty$ up to $R_L = 20\ k\Omega$ is $\leqslant 1$ V.

4. The suppression of subharmonics, relative to V_{QLR}, is $\geqslant 50$ dB.

Type	Ordering code
SAJ 410	Q 67100–J 630
SAJ 410 A	Q 67100–J 771

The SAJ 410 is a static binary frequency divider in MOS depletion technology (double ion-implantation). It is particularly suited for an application in electronic organs.

Special properties

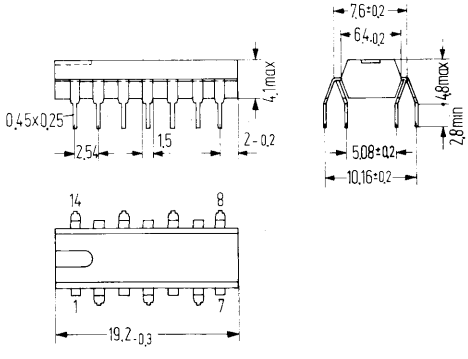
- Pin-compatible to the SAJ 110 and SAJ 210
- Connection of resistors or an auxiliary voltage is not required at the outputs
- Low differential output resistance in both switching states
- Automatic power-on-reset
- Protective structures at all inputs and outputs

Applications

- Electronic organs
- Timing relays
- Frequency dividers
- Counters
- Delay functions

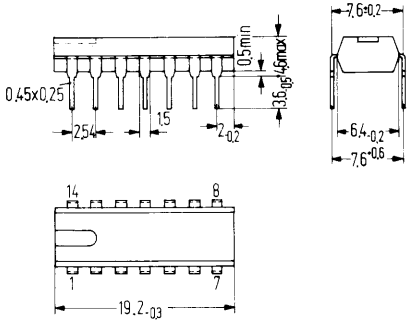
Package outlines

SAJ 410



Plastic plug in package
similar to 20 A 14 DIN 41866
(14 pins QIL)
Weight approx. 1.1 g

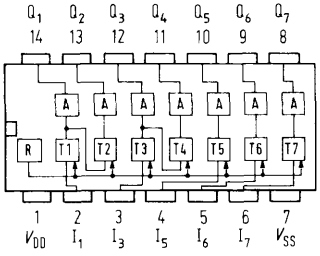
SAJ 410 A



Plastic plug in package
20 A 14 DIN 41866
(14 pins DIL)
Weight approx. 1.1 g

Block diagram and pin connections

Top view



T1 . . . T7 = divider stage 2:1
A = output stage
R = automatic reset

Maximum ratings

		Lower limit B	Upper limit A	Unit
Voltage at all connections (reference V_{SS} = 0 V)	V	−15	0.3	V
Output current per stage	I_Q	−3.5	3.5	mA
Ambient operating temperature	T_{amb}	−25	+70	°C
Storage temperature	T_S	−55	+125	°C

Operating characteristics per stage

(T_{amb} = 25°C)

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}		−14.4	−9.6	V
Supply current at					
output low	I_{DD}	V_{DD} = −12 V	−7	−3	mA
output high	I_{DD}	V_{DD} = −12 V	−7	−3	mA
L-input voltage	V_{IL}			−5	V
H-input voltage	V_{IH}		−1.2		V
Input resistance	R_I		1		MΩ
Input frequency	f_I			100	kHz
Transition time	t_{TI}			40	µs
Differential					
output resistance	R_Q	V_{DD} = −12 V		800	Ω
L-output voltage	V_{QL}	V_{DD} = −12 V		−9	V
H-output voltage	V_{QH}	V_{DD} = −12 V	−1		V

The output changes state with the LH-transition of the input signal.

Reset

Applying the supply voltage V_{DD} causes a reset signal to be produced which puts all outputs at an H-potential. The maximum permissible rate of increase of V_{DD} is 10 V/3 µs. If the reset action has to be absolutely ensured, no LH-transitions must occur at the inputs during the reset operation. The reset has been completed when the supply voltage reaches the operating level.

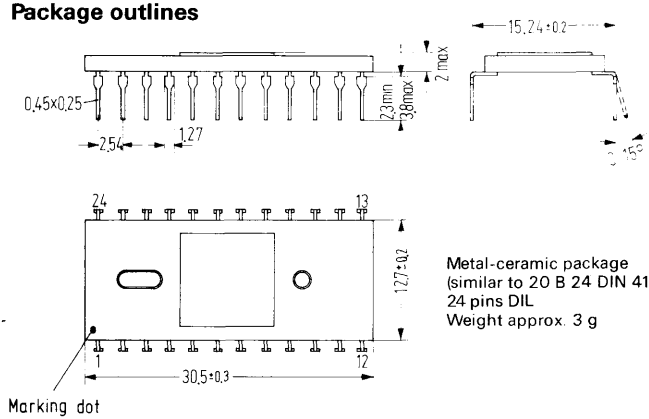
MOS-Circuits for Industrial Applications

Type	Ordering code
S 120 A 3	Q 67100–Z 4

The S 120 A 3 is a highly integrated MOS circuit in p-channel high voltage technology with the following properties:

- Dial-pulse generator for indirect number selection
- Pulse generation integrated
- Inputs BCD-coded
- Single operation or combination with S 121 B possible

Package outlines



Metal-ceramic package
(similar to 20 B 24 DIN 41866)
24 pins DIL
Weight approx. 3 g

Brief description

In connection with the S 121 B, the circuit is suited for indirect number selection. At its input the circuit is BCD-coded. It has the functions of clock generation and dial-pulse generation. With appropriate external connections, single application is possible.
I_{stop} (pin 24) on L-level: Normal operation (output of all digits with preset interval until memory is empty).
When I_{stop} is set to an H-level during the nth digit: Pulse sequence for nth digit is produced completely, further pulse output blocked.
When later I_{stop} assumes an L-level: Generation of the remaining digits until memory is empty; this process will not start before a delay of O . . . 1600 ms.

Operation at clock frequency f_T

Maximum permissible clock frequency f_{Tmax} = 50 kHz (t'= 20 µs)

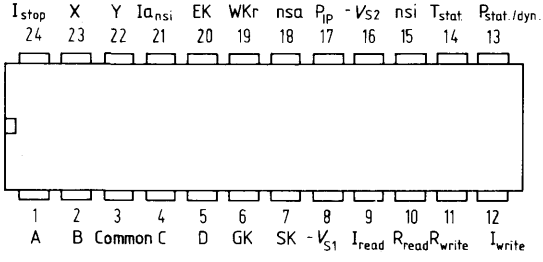
Minimum permissible clock frequency f_{Tmin} = 10 kHz (t'=100 µs)

The corresponding times $\tau'1 \ldots \tau'5$, $\tau'8$, $\tau'9$ and $t'0 \ldots t'8$ may be calculated according to the following formula:

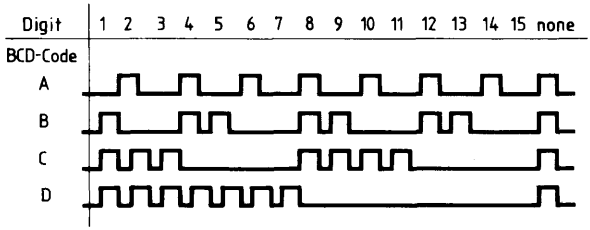
$$\tau'n = \frac{f_o}{f_T} \tau n \text{ and } t'n = \frac{f_o}{f_T} tn$$

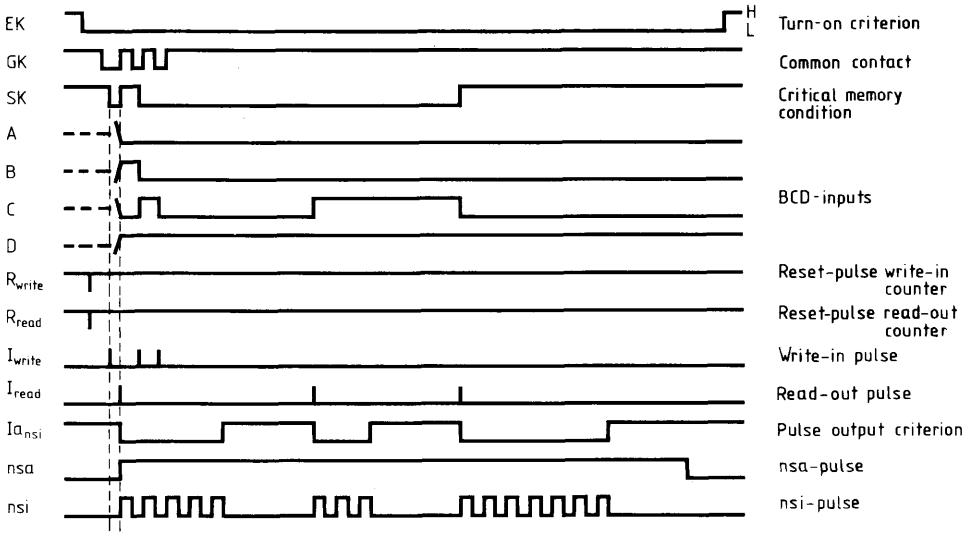
The open inputs are connected to an H- or L-level.

Pin connections, top view

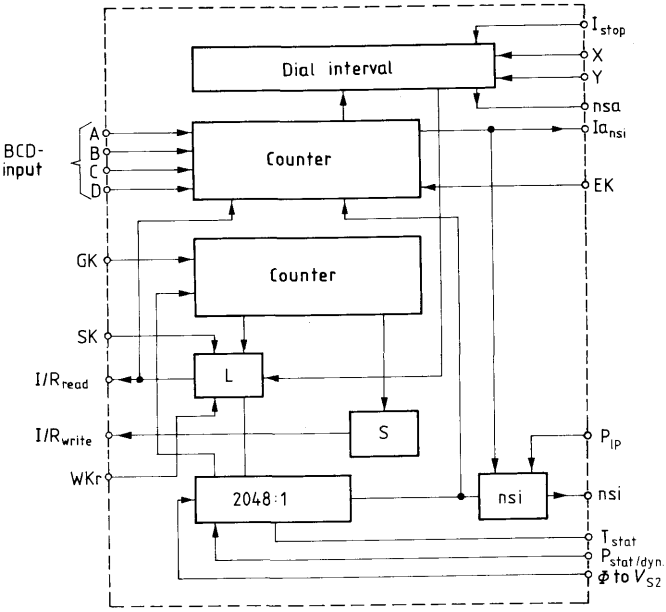


Timing diagram





Block diagram



Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	$V_{S1} = V_{S2}$	−30	0.3	V
Input voltage	V_I	V_{S1}	0.3	V
Output current	$-I_Q$		10	mA
Ambient temperature	T_{amb}	−25	+85	°C
Storage temperature	T_S	−55	+125	°C
Power dissipation	P_{tot}		400	mW
Load capacitance	C_O		50	pF

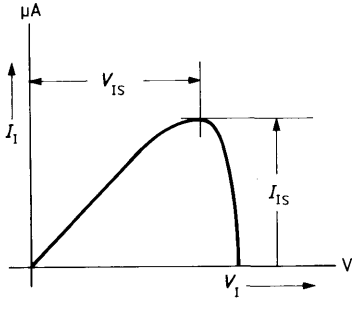
Operating characteristics

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Ambient operating temperature range	T_{amb}				70	°C
Supply voltage		$V_{S1} = V_{S2}$ quasistatic f_O = 20.48 kHz t_p = 1 µs	−27		−23	V
	V_{S1}		−27		−23	V
	V_{S2}		−27		−23	V

Static operating characteristics (all voltages referred to V = 0 V)

Power dissipation		$V_{S1} = V_{S2} = -25$ V			165	mW
		$V_{S1} = V_{S2} = -27$ V outputs unloaded		100	190	mW
		$V_{S1} = -27$ V $V_{S2} = -27$ V clocked t_p = 1 µs f_O = 20.48 kHz		7	10	mW
		$V_{S1} = -27$ V $V_{S2} = -27$ V clocked duty cycle 1:1 f_O = 20.48 kHz			95	mW
Supply current	I_{S1}	$V_{S1} = V_{S2} = -25$ V			6	mA
	I_{S2}				1	mA
Inputs with Schmitt-trigger						
Input I_{stop} and EK	V_{IH}		−2			V
(pin No. 24 and 20)	I_{IH}	$V_{IH} = -2$ V			150	µA
	V_{IL}		−27		10	V
	I_{IL}	$V_{IL} = -27$ V			10	µA
Input threshold	V_{IS}	I_{Imax} = 250 µA	−8	−4	−3	V

Input current $I_I = f(V_I)$



Static operating characteristics

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Input without Schmitt-trigger	V_{IH}		−2			V
	I_{IH}	V_{IH} = −2 V			10	µA
	V_{IL}		−27		−10	V
	I_{IL}	V_{IL} = −27 V			10	µA
Outputs	V_{QL}	I_{QL} = 0 µA			10	V
		I_{QL} = 100 µA			9	V
	V_{QH}	I_{QH} = 100 µA	−1			V
Outputs T_{stat}		quasistatic operation				
	V_{QL}	I_{QL} = 0	V_{S1}		10	V
	V_{QL}	I_{QL} = 25 µA	V_{S1}		9	V
	V_{QH}	I_{QH} = 25 µA	−1			V

Dynamic operating characteristics

		Lower limit B	Typ.	Upper limit A	Unit
Quasistatic operation with S 121 A or B					
Voltage $V_{S\,2}$, f_0 = 20.48 kHz (t_0 = 49 µs)					
Clock amplitude		−23	−25	−27	V
Clock pulse duration	t_P	1			µs
Clock rise-fall	t_V			*400*	µs
Pulse widths					
GK	t_1	20			ms
R_{write}	t_2		6.25		ms
R_{read}	t_3		6.25		ms
I_{write}	t_4		3.12		ms
I_{read}	t_5	3.12		6.25	ms
Dial pulse					
Pulse/pause 1:1	t_6		50		ms
10:6	t_6		62.5		ms
Dial pause					
Pulse/pause 1:1	t_7		50		ms
10:6	t_7		37.5		ms
Dial interval (X = L, Y = L)	t_8		412.5		ms
(X = L, Y = H)	t_8		612.5		ms
(X = H, Y = L)	t_8		812.5		ms
(X = H, Y = H)	t_8		1512.5		ms
Pulse intervals					
GK–GK	τ_9	3			ms
EK–GK	τ_1				
GK–R_{write}	τ_2	3.12		6.25	ms
GK–R_{read}	τ_3	3.12		6.25	ms
R_{write}–I_{write}	τ_4		3.12		ms
I_{write}–I_{read}	τ_5	6.25		25	ms
I_{write}–nsa t_p = 1 µs	τ_6		25	500	µs
I_{read}–nsi (1st pulse)	τ_7			500	µs
I_{ansi}–nsa (last transition)					
(X = L, Y = L)	τ_8		400		ms
(X = L, Y = H)	τ_8		600		ms
(X = H, Y = L)	τ_8		800		ms
(X = H, Y = H)	τ_8		1500		ms

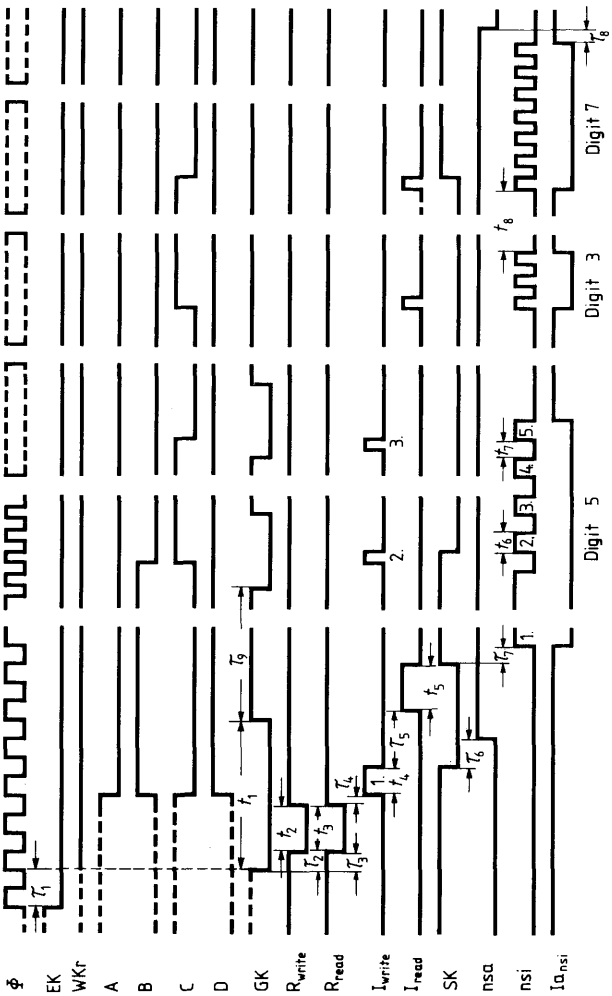
Dynamic operating characteristics

		Lower limit B	Typ.	Upper limit A	Unit
Quasistatic, special operation 1					
f_0 = 20.18 kHz, $t_p = \frac{1}{2 \cdot f_0}$					
Pulse widths					
EK	t'_1	150			µs
I_{read}	t'_2		6.25		ms
Pulse intervals[1]					
EK–WKr	τ'_1	20			µs
WKr–EK	τ'_2	0			µs
EK–WKr	τ'_3	20			µs
WKr–I_{read}	τ'_4	25 µs		32.5	ms

[1]) only when the clock is low at the same time

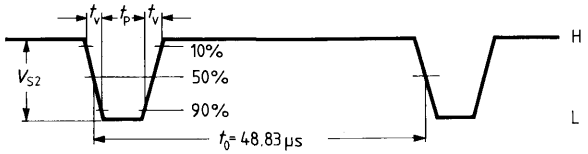
Timing diagram
Operation with S 121 A or B

V_{S2}(≙ø) clocked, f_0 = 20,48 kHz $t_p = \frac{1}{2 \cdot f_0}$

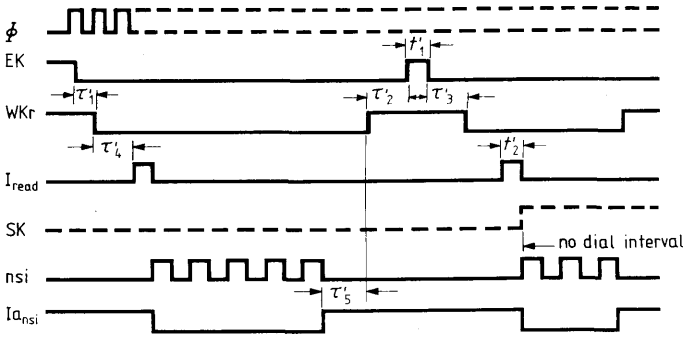


Pulse diagram

Clock voltage $V_{S2}(\hat{=}\phi)$, $f_0 = 20.48$ kHz



For a special operation, $f_0 = 20.48$ kHz, $t_p = \frac{1}{2 \cdot f_0}$

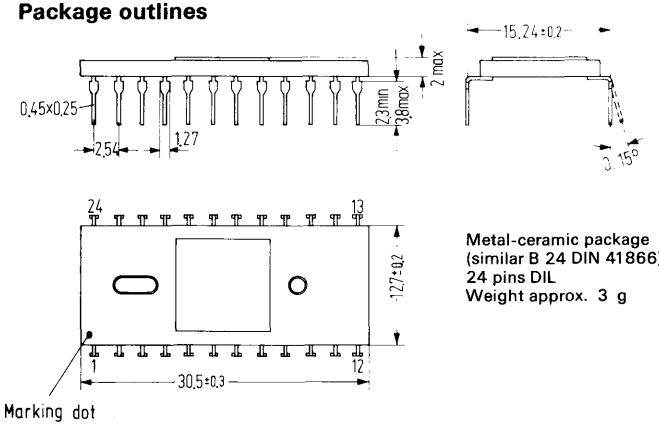


Type	Ordering code
S 121 B	Q 67100–Y 161

The S 121 B is a highly integrated MOS-circuit in p-channel high-voltage technology with the following properties:

- 16 x 4-bit memory for indirect push button dialling
- BCD-coded inputs
- Integrated write and read counter with comparator
- Memory contents is kept
- Combination with S 120 A 3 or single use

Package outlines



Metal-ceramic package
(similar B 24 DIN 41866)
24 pins DIL
Weight approx. 3 g

Brief description

The circuit can be used for indirect dialling together with the circuit S 120 A 3.
Circuit S 121 B is used for BCD-code. Type S 121 A has an MFV-coding at its input.
The circuit consists of a 16 x 4-bit memory, the addressing logic and a read-write-counter-comparator.
With appropriate connections, single application of the circuit is possible.

The data inputs may be floating. All other inputs are to be connected to an H-or L-level.
The memory has 16 storage locations of 4 bits each. Resetting the write or read counter leads to memory location 1.

When using the criterion SK (e.g. in connection with the S 120 A 3), 15 digits will be written in, as the 16th writing pulse causes the counters to be equal. The memory capacity of 16 digits can fully be used if there is at least one read-pulse occurring between the first and the 15th writing pulse.

The memory information will remain after the reading and resetting of the write or read counter.

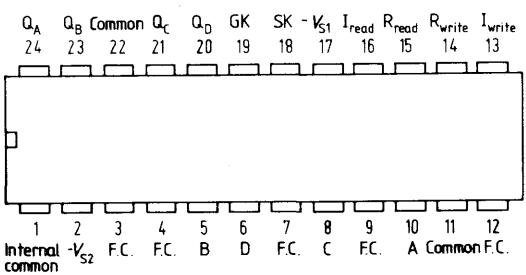
With each writing pulse an information present on the corresponding memory location is replaced. Write or read pulses must overlap with reset pulses possibly occurring at the same time.

Reset, write and read pulses are operating statically (level-effective). The memory condition SK indicates an H-level (corresponding to a logic zero), if after resetting the write and read counter an equal number of write and read pulses has been applied.

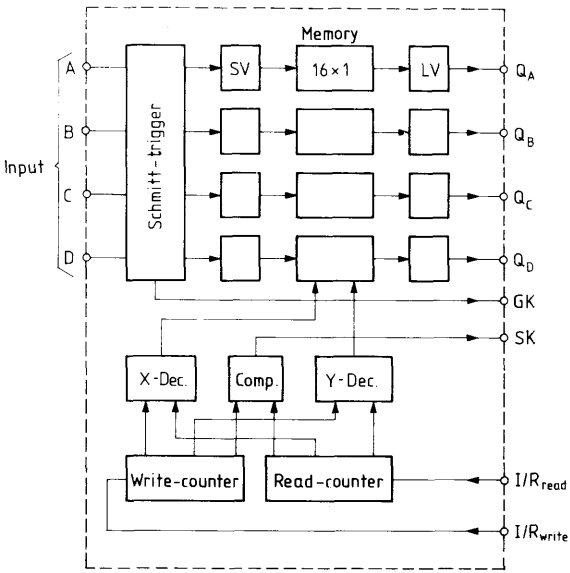
GK (common contact) has a level L (corresponding to a logic 1), if one input (A . . . D) is H.

Even when the read counter remains reset (R_{read} on L-level), new information may be written into the memory.

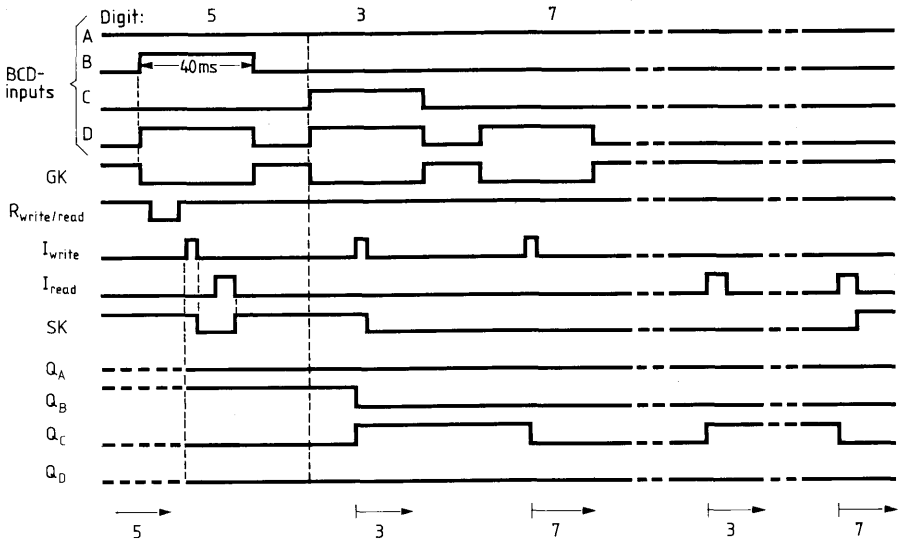
Pin connections, top view



Block diagram



Timing diagram



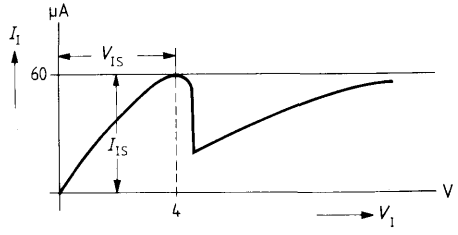
Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	$V_{S1} = V_{S2}$	−30	0.3	V
Input voltage	V_I	V_{S1}	0.3	V
Output current	$-I_Q$		10	mA
Ambient temperature	T_{amb}	−25	+85	°C
Storage temperature	T_S	−55	+125	°C
Power dissipation	P_{tot}		400	mW
Load capacitance	C_0		50	pF

Operating characteristics

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Ambient operating temperature range	T				70	°C
Supply current	I_{S1}	outputs unloaded			10	mA
	I_{S2}				1	mA
Supply voltage		$V_{S1} = V_{S2}$ quasistatic $f_0 = 20.48$ kHz $t_P = 1\ \mu s$	−27		−23	V
		$V_{S1} = V_{S2}$	−27		−23	V
Input with Schmitt-trigger		reg. inputs A . . . D				
H-input voltage	V_{IH}		−2			V
H-input current	I_{IH}	$V_{IH} = -2$ V			150	µA
L-input voltage	V_{IL}		V_{S1}		−9	V
L-input current	I_{IL}	$V_{IL} = -27$ V			250	µA
Input threshold (see figure)	V_{IT}	$I_{IT} \leqq 250\ \mu A$	−8	−4	−3	V
Input without Schmitt-trigger						
H-input voltage	V_{IH}		−2			V
H-input current	I_{IH}	$V_{IH} = -2$ V			10	µA
L-input voltage	V_{IL}	V_{S1}			−9	V
L-input current	I_{IL}	$V_{IL} = -27$ V			10	µA
Outputs Q_A . . . Q_D						
L-output voltage	V_{QL}	$I_{QL} = 0$	V_{S1}		−10	V
L-output voltage	V_{QL}	$I_{QL} = 100\ \mu A$	V_{S1}		−9	V
H-output voltage	V_{QH}	$I_{QH} = 100\ \mu A$	−1			V

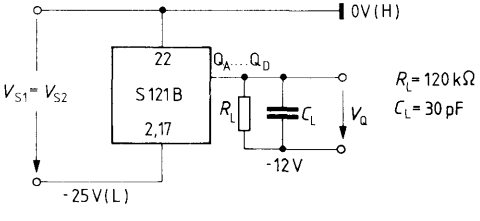
Input current $I_I = f(V_I)$



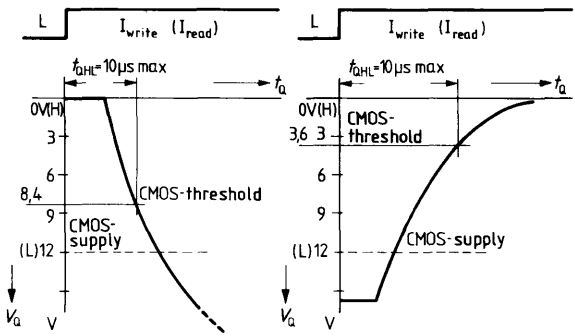
Dynamic operating characteristics

	Lower limit B	Upper limit A	Unit
Static operation with S 120 A 3			
Input timing			
Inputs A . . . D	t'_1	20	ms
Contact bounce	τ'_1	6	ms

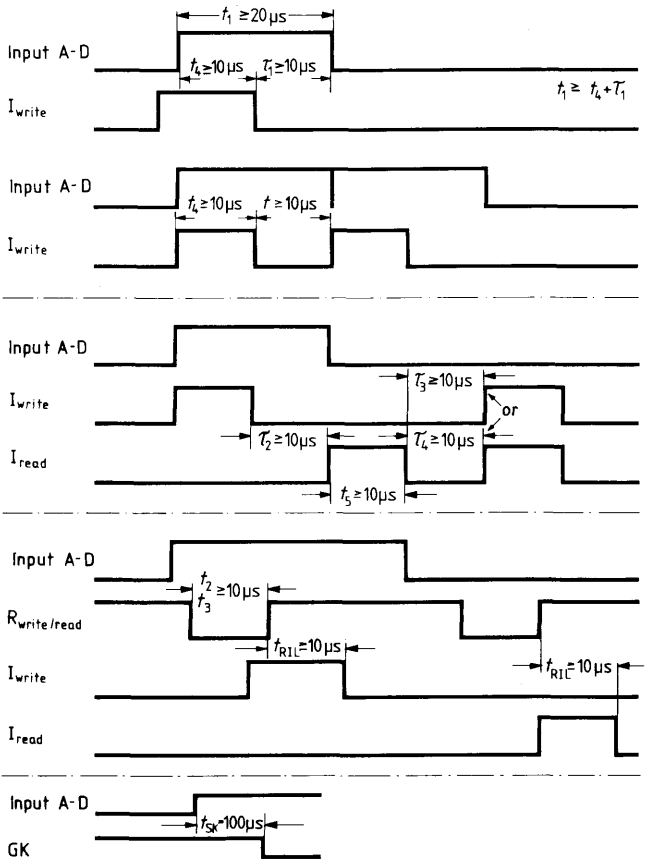
Connection of outputs Q_A . . . Q_D



Output transition timing

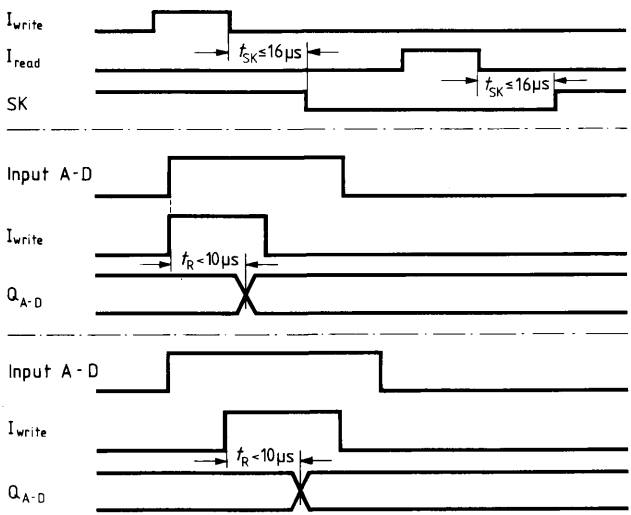


Timing diagram



Time intervals are from 50% of the first pulse voltage to 50% of the second pulse voltage.

Timing diagram



Dynamic operating characteristics

		Lower limit B	Typ.	Upper limit A	Unit
Quasistatic operation with S 120 A 3 f_0 = 20.48 kHz, t_p = 1 µs					
Pulse length Inputs A . . . D	t_1	20	40		ms
Duration of bounce	τ_1			6	ms

Preliminary data

Type	Ordering code
S 178	Q 67100–Z 84

The S 178 is a highly integrated MOS-circuit in p-channel metal-gate technology with enhancement and depletion transistors, with the following technical characteristics:

The **video pulse generator** produces the synchronization, control and erase signals required for the control of cameras, mixers and other equipment. The following signals are generated:

- Strobing signal A
- Synchronization signal S
- Horizontal pulse H
- Vertical pulse V
- Clamping pulse K_t
- Horizontal strobing pulse A (H)
- Double line frequency $H/2$
- One half vertical frequency V_R

} ⟶ $H/2 + V_R$-signal with external signal mixing

Special properties

All pulses are derived digitally from an input frequency, corresponding to a pulse scheme, with a duty cycle of 1:1.

Pulse lengths according to CCIR- and EIA standards.

The following 5 pulse schemes have been programmed in a fixed way (through 3-bit coding and line-number coding):

525 lines (60 Hz) required input frequency 1.008 MHz
625 lines (50 Hz) required input frequency 1.000 MHz
735 lines (60 Hz) required input frequency 1.4112 MHz
875 lines (50 Hz) required input frequency 1.400 MHz
1023 lines (60 Hz) required input frequency 1.96416 MHz

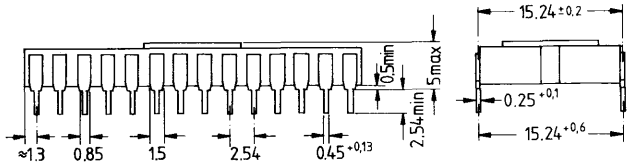
Deviating from the above, any line number between 512 and 1535 lines can be programmed.

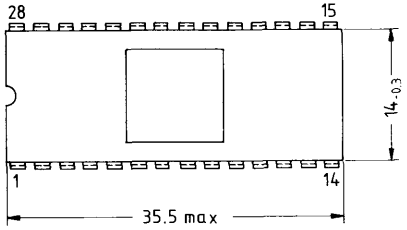
It should be noted, however, that a frame frequency of 50 Hz (partial picture duration 20 ms) or 60 Hz (16.66), respectively, is achieved.

The following relation holds true:

Input frequency f_I = 64 : line period H
= 32 · line number Z · line frequency f_B

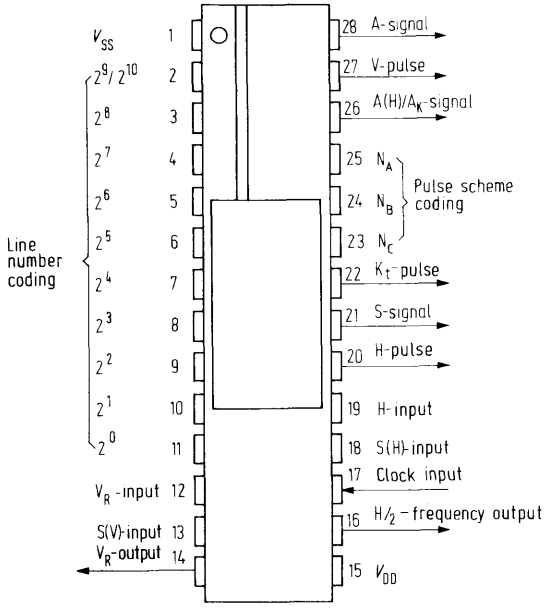
Package outlines





Metal-ceramic package
(28 pins DIL)
Weight approx. 3 g

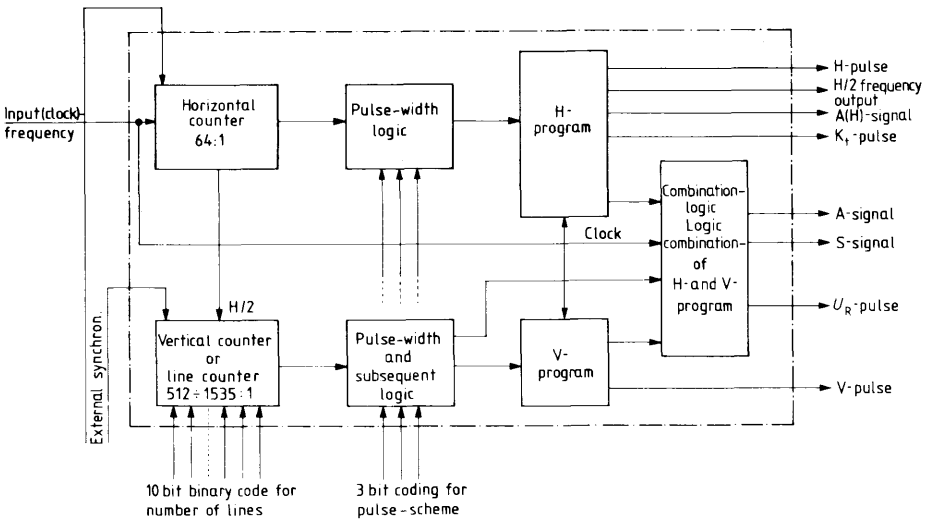
Pin connections, top view



Inputs	Pin-No.	Outputs	Pin-No.
10 inputs for line number coding	2–11	8 outputs for:	
3 inputs for line scheme coding	23–25	A-signal	28
		S-signal	21
2 inputs for external synchronization		A (H) pulses	26
with $H/_2$ + V_R-signal for pulses at H and V_R	19, 12	K_t-pulses	22
2 inputs for external synchronization with		H-pulse	20
S-signal for pulses from S(H) and S(V)	18, 13	V-pulse	27
1 input for the clock frequency	16	$H/_{2\,syn}$– frequency	16
2 inputs for the voltage supply (V_{SS} and V_{DD})	1, 15	V_R-pulse	14

With an appropriate external connection, the $H/_2$ + V_R-signal can be derived by mixing of the $H/_{s\,syn}$ -frequency and the V_R-pulse.

Block diagram



Maximum ratings

			Lower limit B	Upper limit A	Unit
Supply voltage voltage at all pins	relative to V_{SS} = 0 V	V_{DD} U	−12 −20	0.3 0.3	V V
Input current (V_I = 0.3 V; V_{SS} = 0 V)		I_F		100	μA
Storage temperature		T_S	−55	+125	°C
Ambient operating temperature		T_{amb}	0	+75	°C

Operating characteristics: (T_{amb} = 25°C)

a) Operating voltage: $V_{SS}-V_{DD}$ = 10 V ±5%

e.g., if an external TTL-logic is connected using a 0 V and −5 V supply voltage, the MOS-circuit requires a V_{SS} = 0 V and V_{DD} = −10 V supply for direct driving.

b) Current consumption: typically 40 mA

c) Input levels: direct driving with TTL output levels

$V_{SS} \geqq$ log. H $\geqq V_{SS}-1.5$ V
$V_{DD} \leqq$ log. L $\leqq V_{SS}-4.3$ V
fan out ≧1 TTL input load

d) Output level: when loaded with 1 TTL-input (log. H 40 μA; log. L → −1,6 mA)

$V_{SS} \geqq$ log. H $\geqq V_{SS}-2.6$ V
$V_{DD} \leqq$ log. L $\leqq V_{SS}-4.6$ V

e) Rise and fall times: in a range defined by d) ≦100 ns

f) Maximum input frequency: lower limit≧2 MHz typ. 2.8 MHz

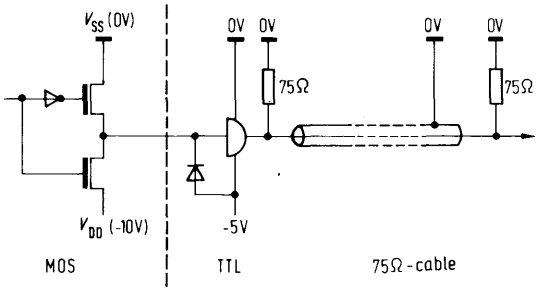
4) Interface to 75Ω-cable

As the outputs of the pulse generator may be loaded with 1 TTL input each as a maximum, a driver stage is required.

Connection according to the circuit diagram shown below.

The additional diode serves as a protection for the TTL-stage against too low an input voltage or against exceeding the permissible power consumption.

As a driver stage for the 75 Ω coaxial cable, the TTL circuit 75 453 (maximum output current 300 mA; pulse delay 11 ns) is recommended.



5) Coding tables

Coding for pulse scheme 1:5

N_A	N_B	N_C		
L	L	L	525 lines	1
L	L	H	625 lines	2
L	H	L	735 lines	3
L	H	H	875 lines	4
H	L	L	1023 lines	5

10-bit dual code for number of lines

1024	512	256	128	64	32	16	8	4	2	1	
2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	connection
L	H	L	L	L	L	L	H	H	L	H	525 lines
L	H	L	L	H	H	H	L	L	L	H	625 lines
L	H	L	H	H	L	H	H	H	H	H	735 lines
L	H	H	L	H	H	L	H	L	H	H	875 lines
L	H	H	H	H	H	H	H	H	H	H	1023 lines

In addition, any other line number may be programmed; however, because of the combination of 2^9 and 2^{10} required to form one input, there is a limitation to 512:1535 lines.

When programming an even line number, the intermediate line is skipped.

1) Description of function

The main units of the pulse generator are horizontal and vertical counters (see block diagram). The horizontal counter, with a counting ratio 64:1, divides the input frequency down to double the line frequency $H/_2$.

An additional logic ensures that in the moment of turn-on, or due to a noise pulse, no undefined condition of the counter flipflops can occur.

The multiples of the input frequency, programmed for all line schemes, are derived from coincidence of the counter; thereby, all pulses are created one clock period ahead of time or pre-synchronized.

Post-synchronization is done with the following clock pulse transition, immediately at the output. Consequently, delays caused by the finite switching speed of the circuit elements are eliminated. Reference transition for all pulses is $H/_2$ syn.

The vertical counter, designed as an 11-bit asynchronous counter, is driven with double the line frequency $H/_2$. All pulses derived from this frequency are a definite integer-multiple of $H/_2$ and occur delayed with respect to this frequency, however, before $H/_2$ syn. Thereby the later-occuring post-synchronization of $H/_2$ syn. is made possible as well.

The vertical counter can be programmed externally for a particular line number. This is done by comparing the externally coded line number with the counter position, in the case of equality internally resetting it and starting anew with the following $H/_2$-transition.
As external programming has been done for the line number of the complete picture, however, the counter is operated with double the line number, the vertical signals will occur per partial picture.

Through the external 3-bit coding, programming is done internally for the chosen pulse-scheme, i.e. the corresponding circuit elements for the realization of the H-and V program are activated.

The pulses are subsequently either directly connected to the outside or mixed appropriately according to the 3-bit-code in the combination-logic and strobed. In any case, a post-synchronization is previously done with the clock-transition. Starting of all pulses and the pulse widths are therefore defined in their timing relative to $H/_2$ syn.

2) External synchronization with $H/_2 + V_R$ or S-signal

For mixing and superposition of the pictures, the BAS-signals of the individual cameras or Video recorders must be synchronized with respect to each other, i.e. they must agree in line- and picture-timing. In the case of external synchronization, the external signal must contain these two components: either the horizontal and vertical frequency (for S-signal, S(H) and (SV)) or the (double-) horizontal- and one-half vertical frequency (for $H/_2 + V_R$).

Of these tow H and V components, short pulses are derived at the beginning of the leading edge, and the horizontal and vertical counters are set to a defined position with these pulses. (Approximate values: H-component $\approx$ 300 ns<pulse period
V-component $\approx$ 1 µs<$H/_2$)

Due to the timing differences of the leading edges of line frequency H and S (H), being 1.5 periods of the input frequency, in one case the horizontal counter would be set to a wrong position. For this reason inputs have been provided for both horizontal components. They can be used to set the counter, depending on the particular component used, to the appropriate position.

The same is valid for the vertical components of $H/_2 + V_R$ and the S signal. The first picture-change pulse follows 2.5 or 3 line periods behind the V_R pulse, depending on the scheme. The two inputs provided for the pulses from V_R or S (V), respectively, and the correspondingly coded line scheme enable the proper setting of the vertical counter. Through the possibility of a defined setting of the counters it is ensured that a proper standard pulse-scheme is obtained at the outputs even in the case of external synchronization involving different phase conditions of the synchronization signals.

Note:

At the time of setting the horizontal counter to a defined position, the phase relation of the input frequency is undefined and consequently the tolerance of the synchronization would be one clock period (i.e. $\leq$1 µs for 625 lines). By means of an external phase synchronization circuit with frequency multiplication, the input clock can be derived from the vertical component and thereby a defined phase relation of the reset pulse achieved relative to the input clock. Hence a common line deviation (jitter) of <20 ns absolute value can be achieved.

3) Control

The pulse generator derives the required pulses from the output frequency. As additionally half a clock period is used for the generation of the pulse widths, and as both the leading and trailing edges are used, an input duty cycle of 1:1 is required.

It is therefore recommended to operate the quartz oscillator used at double the input frequency and to divide it 2:1 with an external stage, thereby achieving an accurate duty cycle of 1:1.

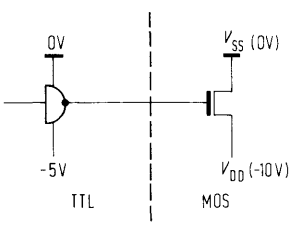
For the line schemes provided the following interrelations hold true:

525 lines	1.008	x 2	→	2.016 MHz
625 lines	1.000	x 2	→	2.000 MHz
735 lines	1.4112	x 2	→	2.8224 MHz
875 lines	1.400	x 2	→	2.800 MHz
1023 lines	1.96416	x 2	→	3.92832 MHz

All inputs of the pulse generator have been designed to be directly TTL output level compatible. It must be taken care that the positive supply voltage for the MOS-circuit is connected to the positive supply of the TTL logic (for MOS = 10 V, for TTL = 5 V).

Inputs not used must be connected to V_{SS} (log. "H").

Connection diagram



Preliminary data

Type	Ordering code
S 187	Q 67100–Y 199

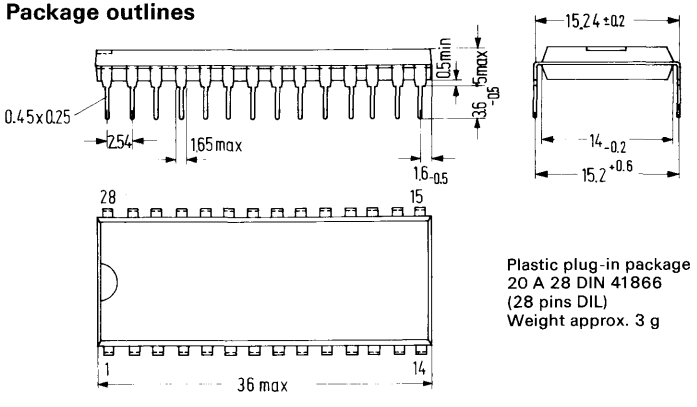
The S 187 is a highly integrated MOS-circuit in p-channel metal-gate technology with enhancement and depletion transistors, featuring the following special technical properties:

- More than 500 000 different frequencies pre-settable
- 8 different reference frequencies pre-settable
- High degree of flexibility through appropriate coding
- High reference input frequency
- Integrated phase comparator
- Simple 10 V supply
- Low power consumption even at high frequencies
- Usable together with diode matrix S 353

Application areas

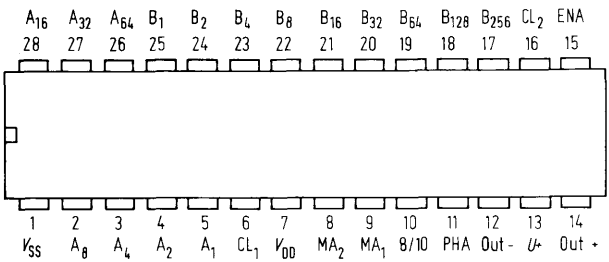
- Multichannel equipment
- Navigation equipment
- Citizen-band radio
- Scanning receiver
- Signal generators

Package outlines



Plastic plug-in package
20 A 28 DIN 41866
(28 pins DIL)
Weight approx. 3 g

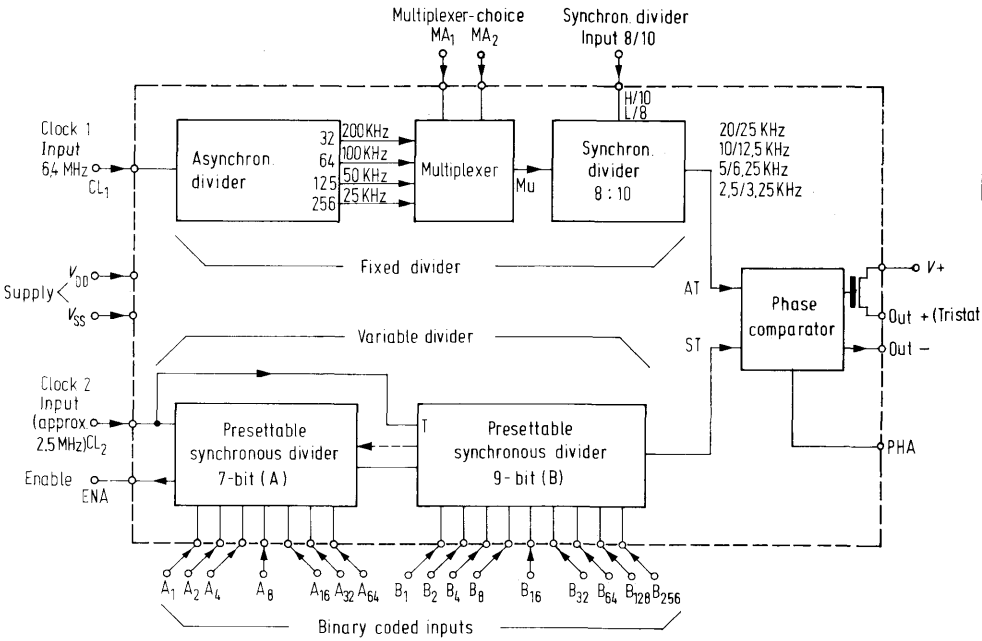
Pin connections, top view



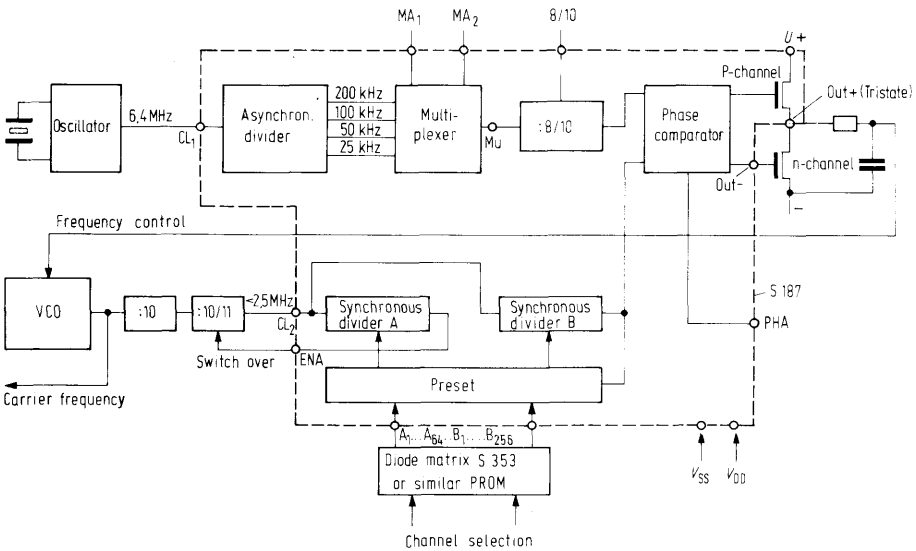
Pin designations:

Inputs			Outputs		
Abbrev.	Pin		Abbrev.	Pin	
A_1	5	Binary coded inputs for pre-settable synchronous divider (A) 7 bits	ENA	15	Release-output
A_2	4		PHA		Phase comparator output
A_4	3		out +	14	Output +
A_8	2		out −	12	Output −
A_{16}	28		$U+$	13	Output for the control of external u-channel transistor
A_{32}	27				
A_{64}	26				
B_1	25	Binary coded inputs for pre-settable synchronous divider (B) 9 bits			
B_2	24				
B_4	23				
B_8	22				
B_{16}	21				
B_{32}	20				
B_{64}	19				
B_{128}	18				
B_{256}	17				
CL_1	6	Clock input 1 for asynchronous divider (max. 6.4 MHz)			
CL_2	16	Clock input 2 for synchronous divider (max. 2.5 MHz)			
8/10	10	Divider setting 8 or 10 for asynchronous divider			
MA_1	9	Multiplexer choice 1 and 2			
MA_2	8				
V_{SS}	1	Supply voltages			
V_{DD}	7				

Block diagram



Block diagram of a carrier frequency generator with S 187



Maximum ratings

			Lower limit B	Upper limit A	Unit
Supply voltage Voltage at all pins	relative to V_{DD} = 0 V	V_{DD} V	15 V 15 V	−0.3 −0.3	V V
Input current (V_I = 0.3 V; V_{DD} = 0 V)		I_F		1	mA
Storage temperature		T_S	−55	+125	°C
Ambient operating temperature		T_{amb}	−20	+70	°C

Operating characteristics: (T_{amb} = 25°C)

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	Used as common and reference voltage	0	0	V
Supply voltage $V_{SS\,typ}$ = 10 V	V_{SS}	V_{DD} = 0V	9	11	V
Current supply	I_{SS}	$I_{SS\,typ}$ = 8 mA		35	mA
Inputs A_1 through A_{64} B_1 through B_{256}, $^8/_{10}$)					
L-resistance H-resistance	R_{IL} R_{IH}	C_{in} = 10 pF to V_{SS} Current input "L" max = ≈ 500 µA (short circuit to V_{DD} at V_{SS} = 10 V)	0 100	3 ∞	kΩ kΩ
Input CL_1 L-input voltage H-input voltage	 V_{IL} V_{IH}	$F_{CI1\,max}$ = 6.5 MHz, $t_a = t_f$ = 25 ns C_{in} = 15 pF to V_{SS} pulse duration 50 ns min.	 V_{DD} V_{SS} −0.5	 V_{SS} −8 V_{SS}	 V V
Input CL_2 L-input voltage H-input voltage	 V_{IL} V_{IH}	$F_{CL\,2\,max}$ = 2.5 MHz, $t_a = t_f$ = 50 ns C_{in} = 25 pF to V_{SS} pulse duration 150 ns min.	 V_{DD} V_{SS} −0.5	 V_{SS} −8 V_{SS}	 V V

Operating characteristics: (T_{amb} = 25°C)

		Test conditions	Lower limit B	Upper limit A	Unit
Inputs MA_1, MA_2					
L-input voltage	V_{IL}	C_{in} = 10 pF	V_{DD}	V_{SS} −8	V
H-input voltage	V_{IH}	to V_{SS}	V_{SS} −0.5	V_{SS}	V
Outputs OUT+, OUT-					
L-output voltage	V_{QL}	I_L = 1 mA, V_{SS} = 10 V	9		V
H-output voltage	V_{QH}	I_H = −1 mA, V_{SS} = 10 V		4	V
	$I_{UK\ max}$	1 µA at T_{amb} = 70 °C			
Output PHA					
L-output voltage	V_{QL}	I_L = 100 µA, V_{SS} = 10 V		6.5	V
H-output voltage	V_{QH}	I_H = −1 mA, V_{SS} = 10 V	6.5		V
Output ENA					
L-output voltage	V_{QL}	open-drain			
H-output voltage	V_{QH}	I_H = 3.5 mA ECL-interface	5		V

Basic functions

The Frequency synthesizer S 187 is used for channel selection in the Carrier Frequency Generator. The carrier frequency is generated by a voltage-controlled oscillator (VCO) and after a **pre-set division** (depending on channel) compared with a crystal-stabilized reference frequency. The output voltage of the frequency comparator controls the VCO.

By appropriate choice of the division, the carrier frequency can be set to a particular multiple of the reference frequency.

Construction and function

See block diagram of a carrier frequency generator including the portion integrated in the S 187.

The following functions are comprised:

a) 8-stage asynchronous divider, input frequency 6.4 MHz max., output frequency selectable 200, 100, 50, 25 kHz.

b) switchable : 8/ : 10-divider,

a) and b) together supply the crystal-stabilized reference frequency (8 possibilities).

c) fully programmable synchronous divider consisting of two interconnected parts; input frequency $\leq$2.5 MHz;

1) 7-stage divider A, pre-settable from : 1 through : 127-division. After completion of the process this divider is stopped. It is reset and triggered by divider B. Consequently it generates the switching signal for a : 10/ : 11 pre-divider, which causes a nonius-kind of division; for this purpose the comparator frequency may be adjusted to a higher value. The switching signal (output ENA) must therefore be synchronized with the input clock (delay <300 nsec.).

2) 9-stage divider B, pre-settable from : 2 through : 512-division. At the end of the process this divider resets itself and divider A. It supplies the divided carrier frequency for the phase-comparator.

d) The phase comparator (see figure) performs the frequency comparison. It possesses 3 possible output combinations (see truth table 1) between which it switches, initiated by 0 → 1 transitions at the inputs (see truth table 2).

In the case of the input frequencies being different, the leading signal switches the output on its side (AT out +, ST out –) to "1"; it remains at this level until the other signal switches it back to "zero".

If both frequencies are equal but different in phase, an output pulse with the width of the phase difference is generated on the leading side with each clock pulse. In the case of both 0 → 1 transitions at the inputs lying within the dwell period, the phase comparator will remain in the "0"-state.

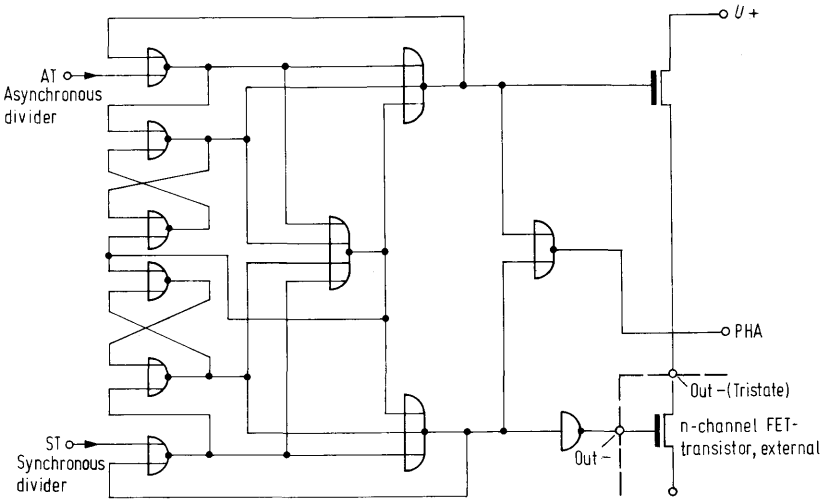
The phase comparator drives a complementary tristate gate, whereby the internal p-channel transistor is driven by the positive-output and the external n-channel transistor from the inverted negative-output. Consequently, the integration capacitor is charged during an H-level, discharged during an L-level. During a O-level its output is connected to a high resistance. Therefore the capacitor voltage, and consequently the frequency of the VCO, changes until the 0 → 1-transitions are within one dwell period of the phase comparator at both inputs.

e) Active-p-function of the programming inputs. The assignment of individual frequencies to particular speech-channels can be done, for example, using a 10 x 16 PROM (diode matrix), which connects the selected programming inputs through a low resistance with a negative potential (L), loading the not-selected ones only with leakage currents (H).

The equivalent worst-case values are: 5 kΩ to V_{DD} (L) or 100 kΩ to V_{DD} (H).

The programming inputs have therefore been provided with an active-p-circuit (see figure), which in the H-condition creates an input voltage of $> V_{SS} - 1$ V and in the L-condition an input voltage of $< V_{DD} + 1$ V. This way various ways of driving the inputs are made possible.

Phase comparator



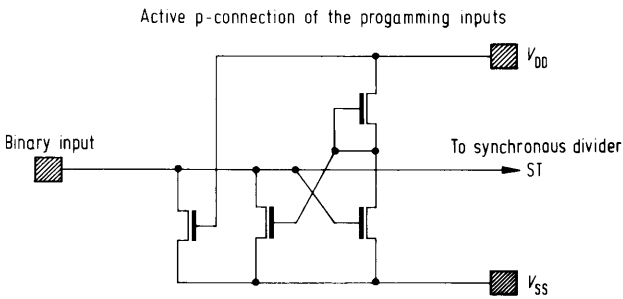
Truth table 1 **Phase comparator**

Condition PHA Phase comparator	Output +	Output –
H	1	0
L	0	1
0	0	0

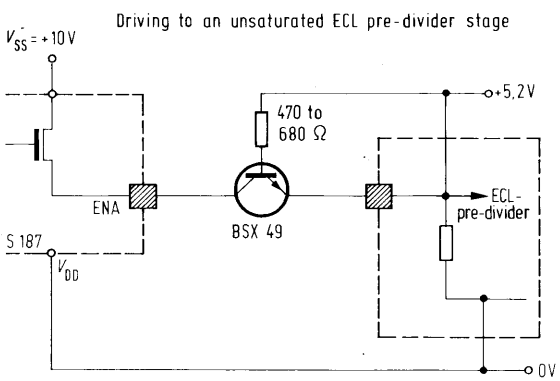
Truth table 2 **Phase comparator**

Output condition PHA Phase comparator	0 → 1-transition at	
	AT Asynchronous divider	ST Synchronous divider
H	H	0
0	H	L
L	0	L

Active-p-connection of the programming inputs



Driving an unsaturated ECL pre-divider stage



Truth tables of dividing ratios for synchronous divider (ST) and asynchronous divider (AT)

a) Inputs 8/10:

H	division by 10
L	division by 8

b) Inputs A_1 through A_{64}:

LSB = A_1
MSB = A_{64}

Condition H LLL LLL corresponds to division by 1

c) Inputs B_1 through B_{256}:

LSB = B_1
MSB = B_{256}

Condition H LLL LLL LL corresponds to division by 1

d) Inputs MA_1 and MA_2:

MA_1	MA_2	Frequency setting at MU
L	L	25 kHz
H	L	50 kHz
L	H	100 kHz
H	H	200 kHz

Preliminary data

Type	Ordering code
S 190	Q 67100-Z 96

The S 190 is a highly integrated MOS-circuit in p-channel metal gate technology, with enhancement and depletion transistors.

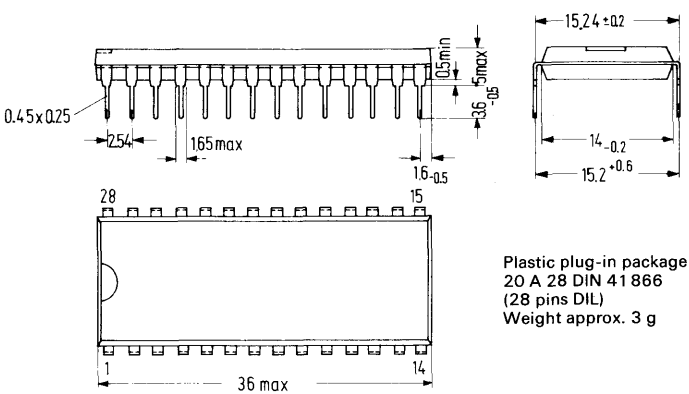
It features the following special technical properties:

- 3¾-digit decade display (±5999 max.)
- Automatic polarity indication
- Automatic range selection
- Range extension
- Overflow indication (blinking)
- 4-decade counter
- Multiplex-BCD-outputs
- Multiplex-oscillator
- Counting-clock oscillator
- Measuring phases for dual-slope method

Particular properties

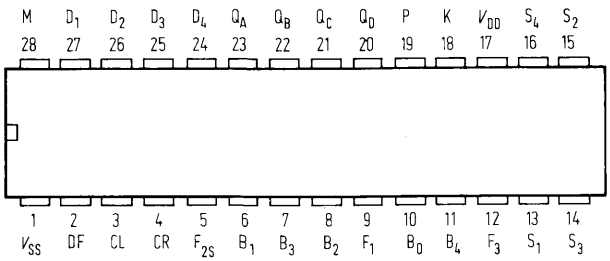
- Low power consumption
- C-MOS compatible
- Fully static

Package outlines



Plastic plug-in package
20 A 28 DIN 41 866
(28 pins DIL)
Weight approx. 3 g

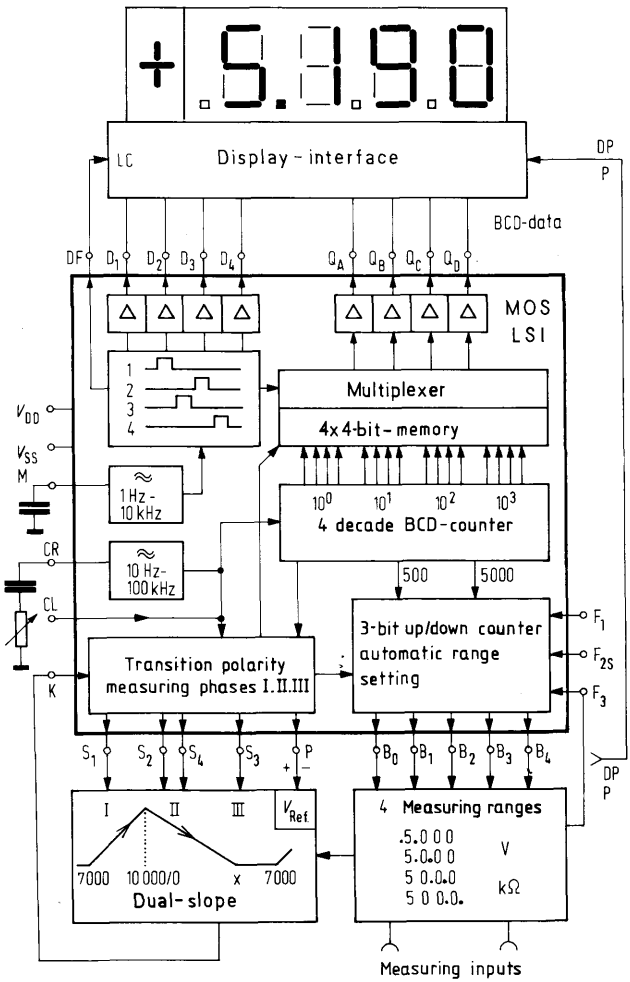
Pin connections, top view



Pin designations

Inputs			Outputs		
Abbrev.	Pin		Abbrev.	Pin	
K	18	Analog input	S_1	13	Measuring phase outputs for dual slope
CR	4	Oscillator-clock connection input for counters and control signals	S_2	15	
			S_3	14	
			S_4	16	
CL	3	External oscillator clock input for counters and control signals	B_0	10	Measuring range outputs
			B_1	6	
			B_2	8	
			B_3	7	
			B_4	11	
M	28	Oscillator clock connection input for multiplexer	P	19	Polarity indication output
			D_1	27	Position selection outputs
			D_2	26	
F_1	9	Measuring range extension inputs	D_3	25	
F_{2S}	5		D_4	24	
F_3	12				
			Q_A	23	BCD-outputs
V_{DD}	17	Supply voltage	Q_B	22	
V_{SS}	1		Q_C	21	
			Q_D	20	
			DF	2	Frequency output for LCD

Block diagram



Maximum ratings

			Lower limit B	Upper limit A	Unit
Supply voltage	referred to	V_{DD}	−20	0.3	V
Voltage at all pins	V_{SS} = 0 V	V	−20	0.3	V
Input current (V_I = 0.3 V; V_{SS} = 0 V)		I_F		1	mA
Storage temperature		T_S	−55	+125	°C
Ambient operating temperature		T_{amb}	−20	+70	°C

Operating characteristics: (T_{amb} = 25°C, unless stated otherwise)

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	Used as common and reference voltage	0	0	V
Supply voltage V_{SStyp} = 12 V	V_{SS}	V_{DD} = 0 V	8	14	V
All inputs except K:		V_{DD} = 0 V (at C_L,			
L-input voltage	V_{IL}	F_{typ} = 30 kHz,	0	V_{SS} −7	V
H-input voltage	V_{IH}	duty-cycle 1:1)	V_{SS}−0.5	V_{SS}	V
K-inputs:					
L-input voltage	V_{IL}		0	V_{SS} −7	V
H-input voltage	V_{IH}		V_{SS} −2	V_{SS}	V
Outputs D_1, D_2, D_3, D_4, Q_A, Q_B, Q_C, Q_D, P:					
L-output voltage	V_{QL}	I_L = 25 µA	0	1	V
H-output voltage	V_{QH}	I_L = −200 µA	V_{SS} −1	V_{SS}	V

		Test conditions	Lower limit B	Upper limit A	Unit
Outputs B_0, B_1, B_2, B_3, B_4, S_1, S_2, S_3, S_4					
L-output voltage	V_{QL}	I_L = 50 µA	0	1	V
H-output voltage	V_{QH}	I_L = −200 µA	V_{SS} −1	V_{SS}	V
Output DF:					
L-output voltage	V_{QL}	I_L = 50 µA	0	1	V
H-output voltage	V_{QH}	I_L = −50 µA F_{typ} = 50 Hz for LCD	V_{SS} −1	V_{SS}	V
Power consumption	P	$V_{DD}-V_{SS}$ = −12 V within power dissipation at the outputs		60	mW
Timing conditions					
Delay time	t_d	between S_3 and K (load = 200 pF, 10 MΩ) measured at 50% of the H-values		4	µs

Oscillator specifications

Counting and control oscillator:

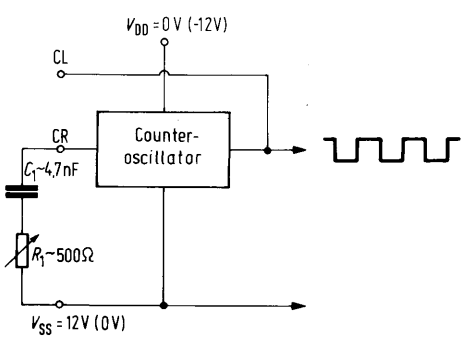
External connections: R, C
Number of pins: 2 (CR, CL)
Frequency parameters:

Parameters	Lower limit A	Typ.	Upper limit B	Unit	Remarks
Frequency f		30	100	kHz	
Frequency stability $F(U) = \frac{\Delta f}{f_G} \cdot 100$		±3		$\frac{\%}{V}$	$\Delta f = f\,(V_{SS} = 12\ V) - f_G$ [2] $T_{amb} = 25°C$ $V_{SS} = 12\ V \pm 1\ V$
Frequency stability $F(T) = \frac{\Delta f}{f_G} \cdot 100$		1) ±0.8	±1	$\frac{\%}{°C}$	$\Delta f = f\,(T = 25°C) - f_G$ $T_{amb} = 0°$ to 70°C $V_{SS} = 12\ V$

[1]) Calculated value
[2]) $f_G = f$ at $V_{SS} = +12\ V$ and $T_{amb} = 25°C$

Operating modes:

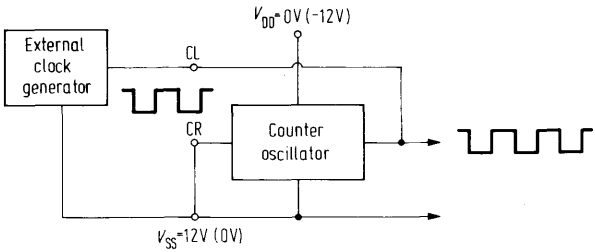
Connection 1



Input CL open

The oscillator drives the decade counter

Connection 2

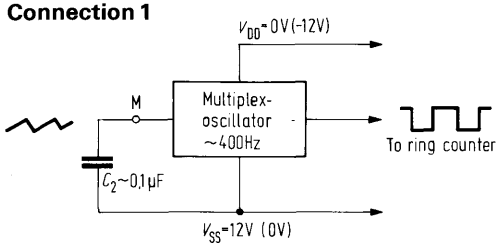


Input CR connected to V_{SS}
Input CL: External clock
The oscillator becomes ineffective and the decade counter is driven externally.

Multiplex oscillator:

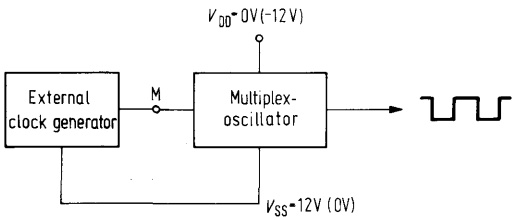
External connection: R, C
Number of pins: 1 (M)
Frequency-parameter: f_{typ} = 400 Hz

Connection 1



Multiplex oscillator

Connection 2



Only for testing purposes and $R_I \approx 0$
Clock generator is loaded by M

Functional description S 190

General

The circuit comprises the logic functions for a digital multimeter, on the basis of the dual-slope-methode, with automatic range switching.

By means of four measuring-range outputs, small units with $3^3/_4$ digits (compare block diagram page 131) and four measuring ranges can be realized without additional external components for the range selection. By switching the range logic, up to eight different measuring ranges can be switched automatically; however, decoding of these ranges must be done externally.

Due to the low power consumption of the S 190 (60 mW), use of a liquid-crystal display permits the design of small units operated by batteries economically.

The maximum display is 6000. 6000 steps mean a relatively small analog circuit requirement, however, they permit the measuring of voltages between 100 µV and 600 V in the four measuring ranges. When the highest measuring range is exceeded, the value 6000 is displayed. Through an additional blinking circuit, which does not require an additional connection pin, the user is made aware of the measuring range being exceeded.

Function

The block diagram shows a simple unit with four automatically selected measuring ranges. The external analog portion consists of only the analog amplifiers, reference voltage source and the analog switches for the measuring phase and range switching.
The sequence control and generation of the value measured is done by the S 190. The main portion of the circuit is made up of a four decade BCD-counter which is driven by a counting oscillator contained on the chip, together with an externally connected RC-circuit (according to page 134). (By connecting a clock generator, according to page 135, the counting oscillator may be replaced). At particular periods of timing the contents of the counter is transferred into the 4 x 4-bit memory by means of a strobe pulse derived from the K-input.
The information contained in the memory is transferred by means of a multiplexer in a bit-parallel mode to outputs Q_A through Q_D, whereby outputs D_1 through D_4 indicate the just transferred decimal place ($Q_A \triangleq$ LSB, $Q_D \triangleq$ MSB; $D_1 \triangleq$ units digit, $D_4 \triangleq$ thousands digit, active condition = high level). To ensure reliable driving of the memories in the display interface, e.g. liquid crystal display, the correct BCD-information is maintained at the Q-outputs until after the end of the active condition of the D-outputs. The indication of decimal position occurs in the sequence 1-3-2-4, to avoid flickering when the display units are driven directly.
For the generation of scan-frequency for the multiplexer a second oscillator has been provided on the S 190 (external connection page 135).
Replacement by an external clock generator is possible (compare page 136) but should be used only for testing purposes. The display frequency DF of about 50 Hz required by liquid crystal displays is also derived from the multiplex oscillator.

Measuring sequence

The measuring sequence is also controlled by the BCD-counter, through measuring-phase outputs S_1 through S_4 (compare timing diagram and principle circuit diagram on page 139).

Phase I, integration of measuring voltage

The measuring cycle starts at counter position 7000; at this point output S_1 becomes high, whereby the input voltage is switched to the integrator until counter position 0000 has been reached.
At the moment when the counter jumps from 9.9999 to 0000, the signal level of the comparator (input K) is stored. At this moment phase II is started.

Phase II, integration of the reference voltage

Depending on the condition of the comparator, only S_2 or S_4 is activated whereby that reference voltage is switched to the integrator which has a polarity opposite to the previously applied input voltage. With this reference voltage the integrator is reduced until the sensitivity threshold of the comparator has been reached and the signal condition at input K changes. This change of signal activates S_3. The number of counting pulses between counter position 0000 and X is proportional to the measuring voltage. Through the low → high transition of S_3 the counter contents is loaded into the display memory; at this point of time phase III is started.

Measuring sequence

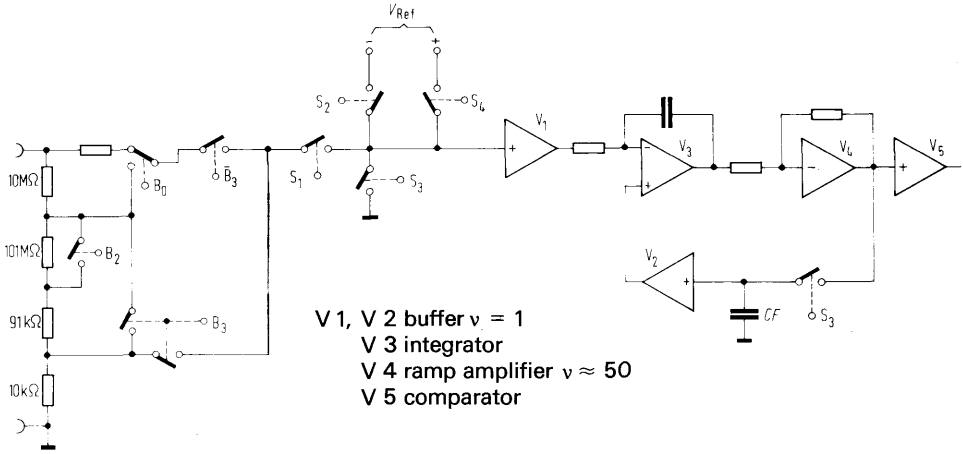
Phase III, zero regulation

In this process the input of the AD-converter is set to zero and the resulting error voltage is stored in capacitor C_F. An error voltage is compensated through a feedback loop. The durration of phase I is determined by the counter frequency and the fixed number of 3000 counting steps. For a 30 kHz counting frequency, phase I lasts exactly 100 ms. The longer the integration time is, the better the noise voltages superimposed on the measuring signal are suppressed. If the duration of the noise voltage period is contained in the integration time as an even number, this noise is suppressed completely. As noise voltages can be expected to occur especially at line frequency, 100 ms integration time constitute a favourable compromise between integration time and noise voltage suppression. The duration of phase II is determined by the level of measuring voltage. If the measuring voltage is too large, the integrator cannot be discharged during the 6000 counting steps available as a maximum; consequently, at step 6000 phase III is initiated. Hence, the integrator will have assumed the correct starting position at the beginning of phase I which follows.
For excessive measuring voltages the display is therefore 6000. In order to bring the incorrectness of this display to the user's attention, the pseudo-decade HHHH is made active at the outputs, synchronously to signal S_1; thereby a blinking effect of approx. 3 Hz is obtained.

Automatic range switching

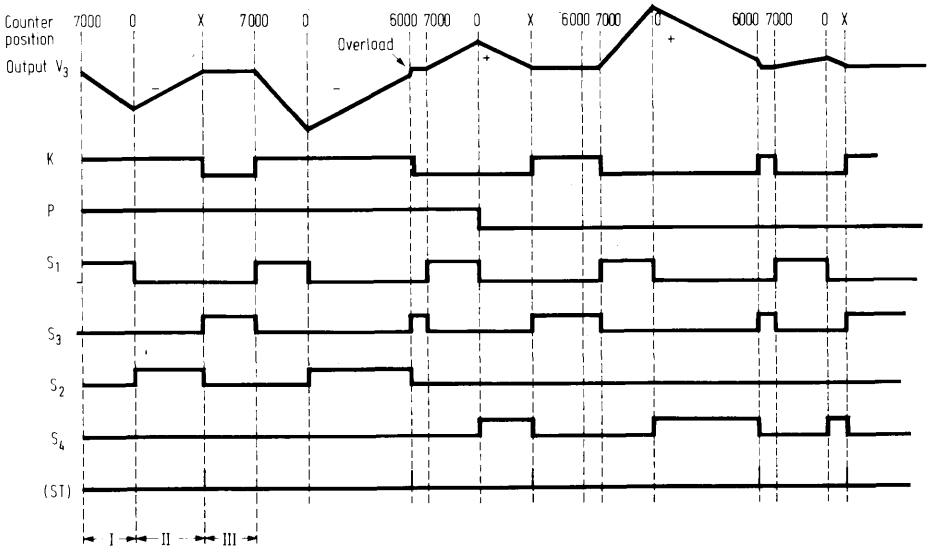
The measuring range is changed whenever the measuring result has been $\geq$5500 or <500. For n $\geq$5500 the range counter (3 bit up down counter) is stepped up by one count, for n <500 stepped down by one, whereby the counter is blocked on the lowest or highest digit position, respectively. The range selection can be controlled through control inputs F_1, F_{2S} and F_3.
When the control inputs F_1, F_{2S} and F_3 are in a low condition, the counter can move within the lower 5 positions up or down. Should it be in a higher position, it can step only downward until the "free zone" has been reached; the decoder produces correct values also for counter positions outside the "free zone", so that the system adjusts itself.
Through an H-signal at input F_1 the correlation between the counter position and decoder output can be changed. Thereby it is made possible to perform range setting for the voltage and resistance ranges and the control of the decimal point in a simple unit with four measuring ranges without external decoding. Input F_3 is used to set counter to the highest level. The highest measuring range is activated and maintained as long as F_3 is kept at a high level. For example, thereby the range 500.0 V is activated, which is an advantage for quick overview-measurements.
A high level at input F_{2S} has the effect that the outputs of the range counter are directly transferred to the outputs; 8 different ranges are then available which must be decoded by external means. In the case of F_{2S} = H the "free zone" of the counter is expanded to the full counting range; the prevention of "running wild" is maintained.

Basic circuit of the analog divider (example usable for a simple unit)



V 1, V 2 buffer $\nu = 1$
V 3 integrator
V 4 ramp amplifier $\nu \approx 50$
V 5 comparator

Timing diagram AD-converter



Phase { I Integration of measuring value
II Integration of reference voltage
III Zero regulation

Automatic range selection
Truth table

Nr.	Q_3	Q_2	Q_1	F_1	F_{2S}	F_3	B_0	B_1	B_2	B_3	B_4
0	L	L	L	L	L	L	H				
1	L	L	H	L	L	L		H			
2	L	H	L	L	L	L			H		
3	L	H	H	L	L	L				H	
4	H	L	L	L	L	L				H	H
5	H	L	H	L	L	L				H	H
6	H	H	L	L	L	L				H	H
7	H	H	H	L	L	L				H	H
10	L	L	L	H	L	L		H			
11	L	L	H	H	L	L		H			
12	L	H	L	H	L	L			H		
13	L	H	H	H	L	L				H	
14	H	L	L	H	L	L					H
15	H	L	H	H	L	L					H
16	H	H	L	H	L	L					H
17	H	H	H	H	L	L					H
2 X	Q_3	Q_2	Q_1	X	H	L	X	Q_1	X	Q_2	Q_3
30	H	H	H	L	L	H				H	H
31	H	H	H	H	L	H					H
32	H	H	H	X	H	H	X	H	X	H	H

Q_1, Q_2, Q_3 internal outputs of the up/down counter

The truth table for setting the measuring ranges should be understood as follows:

The range outputs B_0 . . . B_4 are intended to directly drive the five possible decimal places of a 4-decade display. Simple units with 4 measuring ranges have been taken into consideration. For example, in the case of voltages the measuring ranges with F_1 = low are:

B_0	.5000 V
B_1	5.000 V
B_2	50.00 V
B_3	500.0 V

The total measuring range therefore comprises 0.1 mV through 599.9 V.
For resistance measuring, however, F_1 must be high:

B_1	5.000 kΩ
B_2	50.00 kΩ
B_3	500.0 kΩ
B_4	5000. kΩ

The total measuring range therefore comprises 1 Ω through 5.999 MΩ.
Hence, using control input F_1, choice of one of the two groups is basically possible.

The range outputs are also intended to directly drive the appropriate four selection relays without additional logic gating. When the automatic range selection (e.g. after turn-on) has not yet found the correct range, some measuring range is expected to be shown anyway. This side-condition is considered in the truth table of vector Ø . . . 17.

It should be noted, however, that Q_1, Q_2 and Q_3 in the truth table are internal outputs of the internal up/down counter. It is also possible to select one of 5 measuring ranges automatically. To do this the 4th and the 5th measuring range are separated through external gating at F_1 = low (whereby $MB_4 = B_3 \cdot \overline{B_4}$ and $MB_5 = B_4$). MB_4 is measuring range 4, MB_5 is measuring range 5.

$F_{2\,S}$ = high causes an extension to all eight possible measuring ranges. The range selected appears at outputs B_1 (= Q_1), B_3 (= Q_2) and B_4 (= Q_3) dual-coded. Hence, vectors 20-27 of the truth table are fixed.

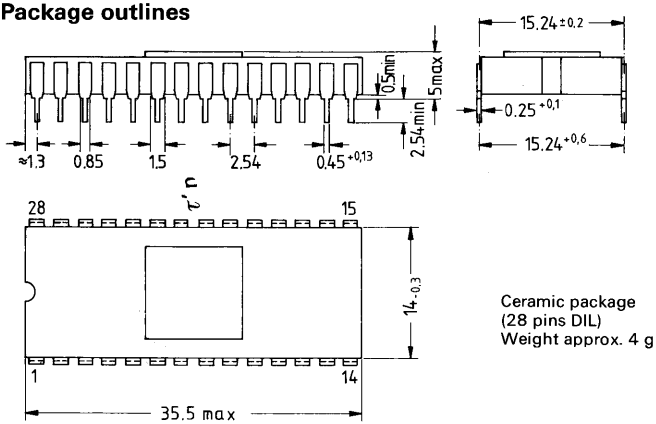
Preliminary information

Type	Ordering code
S 607	Q 67100–Z 108

Technical characteristics

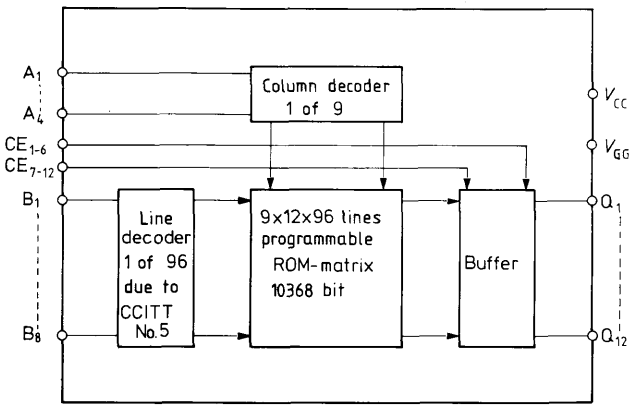
- p-MOS technology with ion implantation
- Supply voltages +5, −12.0 V
- Static inputs TTL-compatible
- Tristate outputs
- Maximum output current loading 1.6 mA, typ. 0.4 mA
- Access time approximately 10 µs
- Power dissipation max. 700 mW
- Operating temperature 0 to 70°C
- Mask-programmable

Package outlines



Ceramic package
(28 pins DIL)
Weight approx. 4 g

Block diagram



Static Frequency Divider 1000:1

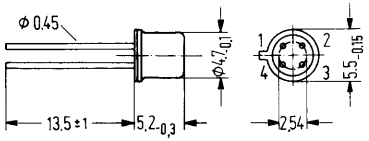
SAJ 131
SAJ 131 A
SAJ 135
SAJ 135 A

Type	Ordering code
SAJ 131	Q 67100-J 126
SAJ 131 A	Q 67100-J 170
SAJ 135	Q 67100-J 127
SAJ 135 A	Q 67100-J 285

Types SAJ 131 and SAJ 135 are static MOS frequency dividers with a dividing ratio 1000:1. Both circuits can be supplied also with a reset input, called SAJ 131 A or SAJ 135 A, respectively.

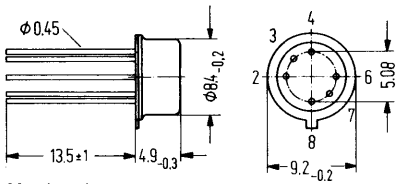
Package outlines

SAJ 131, SAJ 135



Metal package
18 A 4 DIN 41876 (similar to TO-72)
(4 pins)
Weight approx. 0.4 g

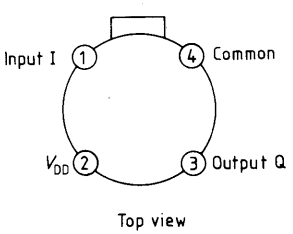
SAJ 131 A, SAJ 135 A



Metal package
5 H 6 DIN 41873 (similar to TO-78)
(6 pins)
Weight approx. 1.1 g

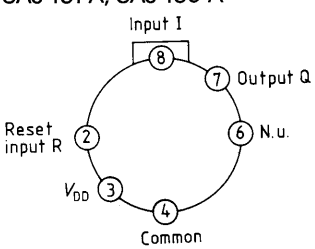
Pin connections

SAJ 131, SAJ 135



Top view

SAJ 131 A, SAJ 135 A



Top view

Maximum ratings

	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	−20	0.3	V
Input voltage	V_I	−20	0.3	V
Output current	I_Q	−2		mA
Ambient operating temperature (range 1)	T_{amb}	0	+70	°C
Ambient operating temperature (range 5)	T_{amb}	−25	+70	°C
Storage temperature	T_S	−55	+125	°C

Static operating characteristics

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}		−19	−17	V
Supply current	I_{DD}		−4		mA
H-input voltage	V_{IH}		−2		V
L-input voltage	V_{IL}			−12	V
H-input voltage at reset input	V_{RH}		−2		V
L-input voltage at reset input	V_{RL}			−12	V
Input resistances	R_I		10		MΩ
H-output voltage	V_{QH}	$I_Q = -1$ mA	−7		V
L-output voltage	V_{QL}			−15	V
H-output current	I_{QH}	$R_Q = -10$ kΩ		−1	mA
L-output current	I_{QL}	$R_Q = -10$ kΩ	−10		µA

Output condition and counter position are not defined after applying supply voltage. In a continuous dividing operation the output is normally L and assumes an H-level after each 1000th input pulse until the next input pulse is received.

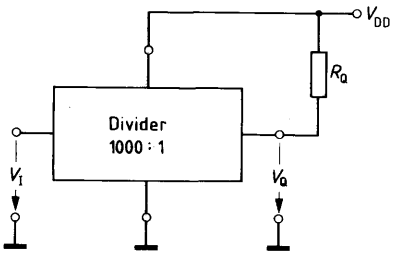
Dynamic operating characteristics

		Test conditions	Lower limit B	Upper limit A	Unit
Information input					
Input frequency	f_I	see figure 4	0	25	kHz
Pulse width	t_{WLI}		10		µs
Pulse dwell	t_{WHI}		15		µs
HL-transition	t_{THLI}			2	µs
LH-transition	t_{TLHI}			2	µs
Information output					
Pulse width	t_{WHQ}		5		µs
Delay time	t_{DLH}			15	µs
HL-transition	t_{THLQ}			5	µs
LH-transition	t_{TLHQ}			5	µs
Reset input					
Pulse width	t_{WLR}		10		µs
HL-transition	t_{THLR}			2	µs
LH-transition	t_{TLHR}			2	µs

Reset input (SAJ 131 A, SAJ 135 A):
The reset signal V_R is dominating, i. e. the output signal is L as long as the reset input is on an H-level. It must have disappeared at least 10 µs before the following LH-transition of an input signal to be counted.
An H output signal is reset to L within 5 µs after application of the reset signal.

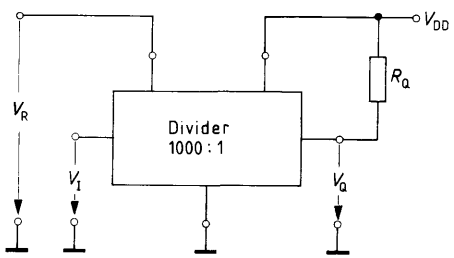
Connection

Fig. 1



SAJ 131, SAJ 135

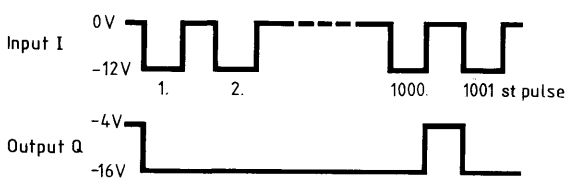
Fig. 2



SAJ 131 A, SAJ 135 A

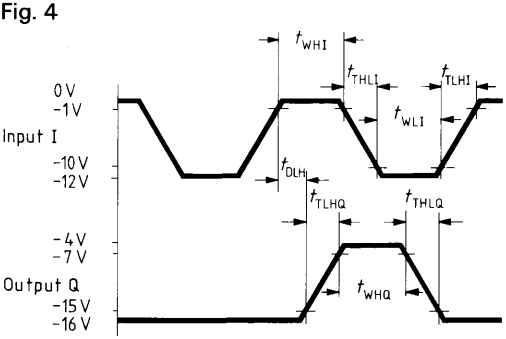
Timing diagram, 1000:1-divider

Fig. 3



Pulse diagram, 1000:1 divider

Fig. 4



Static Frequency Divider 1000:1 in Ion Implantation Technique

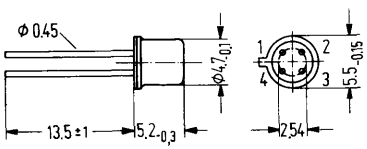
SAJ 131-I
SAJ 131 A-I
SAJ 135-I
SAJ 135 A-I

Type	Ordering code
SAJ 131-I	Q 67100-J 569
SAJ 131 A-I	Q 67100-J 547
SAJ 135-I	Q 67100-J 570
SAJ 135 A-I	Q 67100-J 548

Types SAJ 131-I and SAJ 135-I are static MOS frequency dividers with a dividing ratio 1000:1. Both circuits can also be supplied with reset inputs, called SAJ 131 A-I or SAJ 135 A-I, respectively

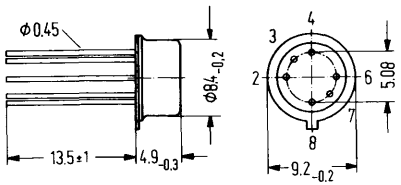
Package outlines

SAJ 131-I, SAJ 135-I



Metal package
18 A 4 DIN 41876 (similar to TO-72)
(4 pins)
Weight approx. 0.4 g

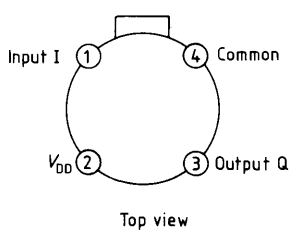
SAJ 131 A-I, SAJ 135 A-I



Metal package
5 H 6 DIN 41873 (similar to TO-78)
(6 pins)
Weight approx. 1.1 g

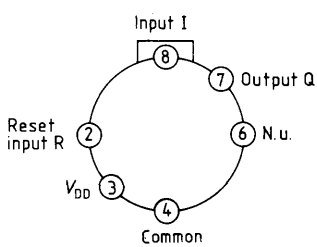
Pin connections

SAJ 131-I, SAJ 135-I



Top view

SAJ 131 A-I, SAJ 135 A-I



Top view

Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	−15	0.3	V
Input voltage	V_I	−15	0.3	V
Output current	I_Q	−1.5	0	mA
Ambient operating temperature (range 1)	T_{amb}	0	+70	°C
Ambient operating temperature (range 2)	T_{amb}	−25	+85	°C
Storage temperature	T_S	−55	+125	°C

Static operating characteristics

		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_{DD}		−12		−9	V
Supply current	I_{DD}	without load resistance	−2	−0.8		mA
H-input voltage	V_{IH}		−1.2		0.3	V
L-input voltage	V_{IL}		−9		−3.5	V
H-input voltage at reset input	V_{RH}		−1.2		0.3	V
L-input voltage at reset input	V_{RL}		−9		−3.5	V
H-output voltage	V_{QH}	R_Q = 10 kΩ	−2.5			V
L-output voltage	V_{QL}	R_Q = 10 kΩ			V_{DD}+0.2	V
H-input resistance	R_{IH}		10			MΩ
L-input resistance	R_{IL}		10			MΩ

Dynamic operating characteristics

Information input (see fig. 4)						
Input frequency	f_I		0		25	kHz
Pulse width	t_{WLI}		10			µs
Pulse dwell	t_{WHI}		15			µs
HL-transition	t_{THLI}				2	µs
LH-transition	t_{TLHI}				2	µs
Information output (see fig. 4)						
Pulse width	t_{WHQ}		5			µs
Delay time	t_{DLH}	C_Q = 10 pF			15	µs
HL-transition	t_{THLQ}	C_Q = 10 pF			5	µs
LH-transition	t_{TLHQ}	C_Q = 10 pF			5	µs
Reset input						
Pulse width	t_{WLR}		10			µs
HL-transition	t_{THLR}				2	µs
LH-transition	t_{TLHR}				2	µs

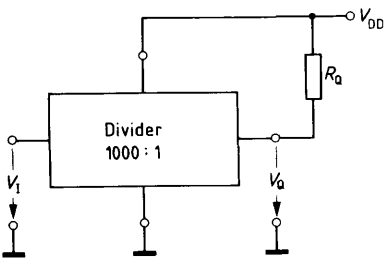
Reset inputs (SAJ 131 A-I, SAJ 135 A-I)

The reset signal V_R is dominating, i. e. the output signal is on an L-level as long as an H-signal is applied to the reset input. It must disappear at least 10 µs before the next LH-transition of an input signal to be counted.

An H output signal is reset to L within 5 µs after applying the reset signal.

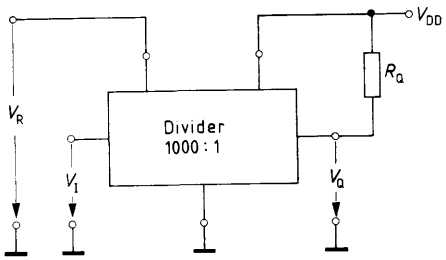
Connections

Fig. 1



SAJ 131-I, SAJ 135-I

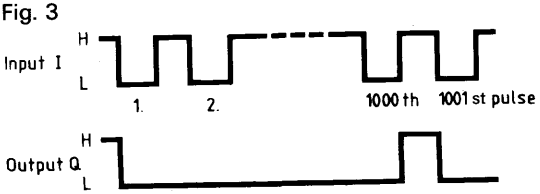
Fig. 2



SAJ 131 A-I, SAJ 135 A-I

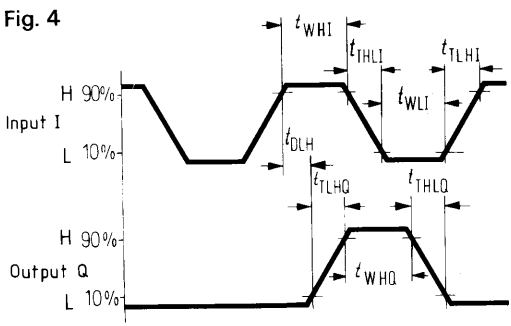
Timing diagram

Fig. 3



Pulse diagram

Fig. 4



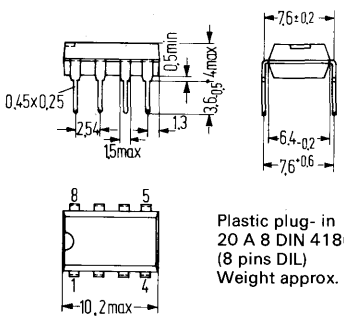
Type	Ordering code
SAJ 141	Q 67100–N 62

The SAJ 141 is an asynchronous counter in MOS depletion technique which generates, at three open-drain outputs, the dividing ratios 1000:1, 100:1, or 10:1 of the input frequency. Counted are the LH-transitions.

The circuit contains a second input with a higher switching threshold for applications in which high noise immunity is required.

A special reset arrangement provides that the first LH-transition appears at the corresponding output not before 10, 100 or 1000 inputs have occured.

Package outlines



Plastic plug- in package
20 A 8 DIN 41866
(8 pins DIL)
Weight approx. 0.7 g

Pin connections

Pin No.	Designation
1	V_{SS}
2	Input I_1
3	Input I_2
4	Reset input R
5	Output Q_2 (100:1)
6	Output Q_3 (1000:1)
7	Output Q_1 (10:1)
8	V_{DD}

Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	−20	0.3	V
Input voltage	V_I	−20	0.3	V
Output current	I_Q	−15	0	mA
Ambient operating temperature (range 1)	T_{amb}	−0	+70	°C
Storage temperature	T_S	−55	+125	°C

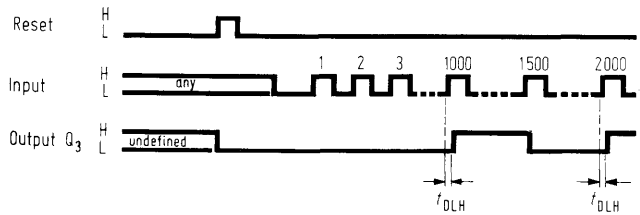
Static operating characteristics (T_{amb} = 25°C)

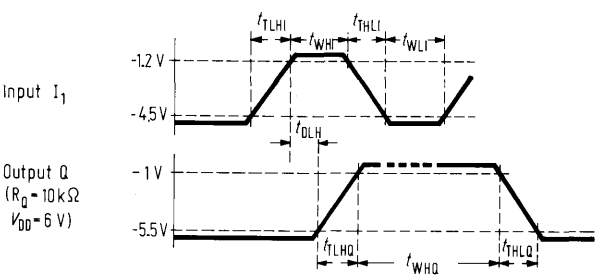
		Test conditions	Lower limit B	Typ.	Upper limit A	Unit
Supply voltage	V_{DD}		−16		−4.75	V
Supply current	I_{DD}	also for	−5	−3		mA
H-input voltage	V_{IH1}	reset	−1.2		0.3	V
L-input voltage	V_{IL1}	input	−16		−4.5	V
H-input voltage	V_{IH2}		−2.5		0.3	V
L-input voltage	V_{IL2}		−16		−8	V
H-input voltage	V_{QH}	R_Q = 10 kΩ	−2			V
L-output voltage	V_{QL}	R_Q = 10 kΩ			V_{DD}+0.3	V
H-input resistance	R_{IH}		10			MΩ
L-input resistance	R_{IL}		10			MΩ
Permissible output current	I_Q		−10			mA

Dynamic operating characteristics

Input frequency	f_I		0		1	MHz
Pulse width	t_{WLI}		450		∞	ns
Pulse dwell	t_{WHI}		450		∞	ns
HL-transition	t_{THLI}				0.3	ms
LH-transition	t_{TLHI}				0.3	ms
at f = 1 MHz, division 10:1						
Pulse width	t_{WHQ}		2			µs
Delay time	t_{DLH}	C_Q = 10 pF		0.8	2	µs
HL-transition time	t_{THLQ}	R_Q = 10 kΩ			3	µs
LH-transition time	t_{TLHQ}			0.4	1	µs

Timing diagram

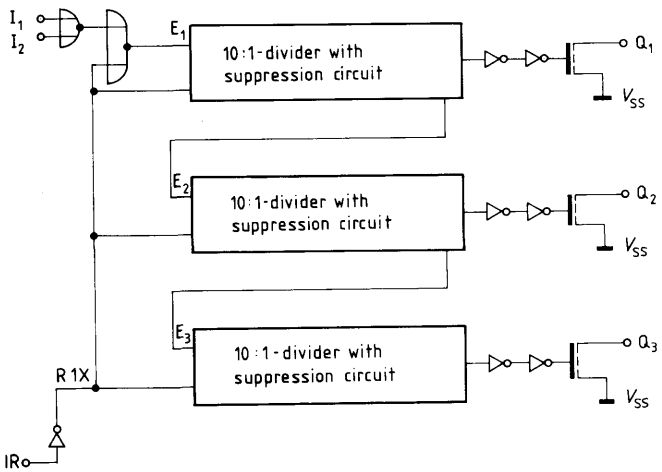




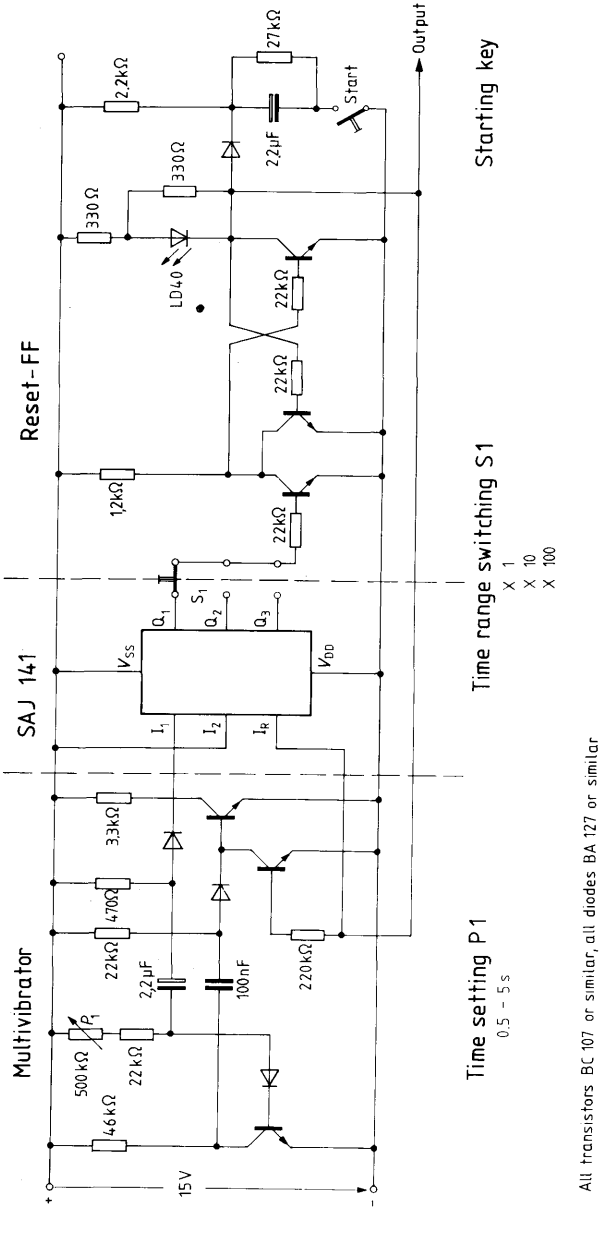
Inputs I_1 and I_2 are gated with each other

Input	Level	Function
I_1	L	I_2 blocked
I_1	H	LH-transitions at I_2 are counted
I_2	L	I_1 blocked
I_2	H	LH-transitions at I_1 are counted

Block diagram



Example of a circuit diagram for a timing pulse generator



Type	Ordering code
SAJ 341 A	Q 67100-J 823

The circuit SAJ 341 A, fabricated in MOS ion-implantation depletion technique, contains the following two main functions essentially:

1. A 4-decade up-counter with count-preset and pre-settable pre-dividers (1:1, 10:1, 100:1, 1000:1, 6000:1).
2. A clock function with output of minutes and hours. As a time basis, a 50 Hz-, 60 Hz- or a 100 Hz-signal can be applied externally.
   Reading of the pre-select-inputs and -output of the BCD display digits is done by multiplexing.

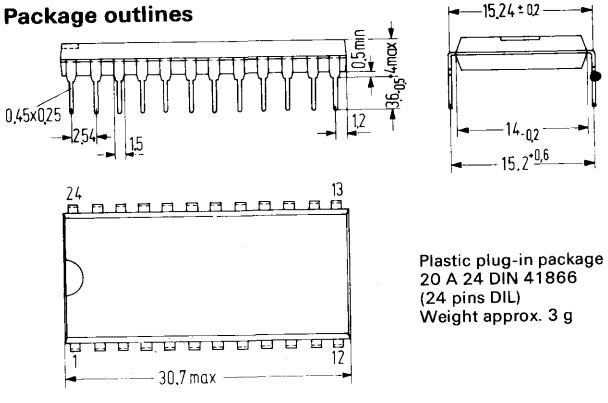
Applications

- Up-counter
- Delay functions
- Pulse-quantity counter
- Time measurement
- Switching clock
- Clock function
- Pre-settable frequency divider
- Digital time switch

Special properties

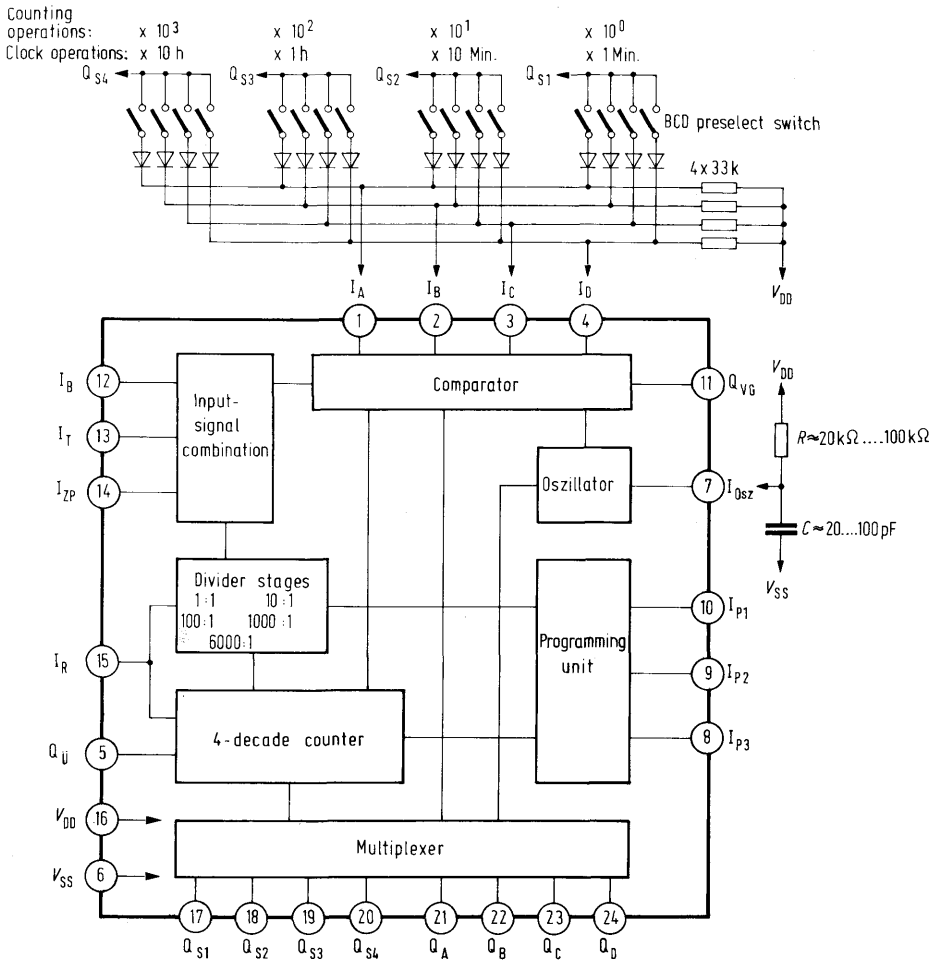
- Low power consumption (max. 200 mW)
- High noise rejection
- Open-drain outputs
- Protection structures at all pins

Package outlines



Plastic plug-in package
20 A 24 DIN 41866
(24 pins DIL)
Weight approx. 3 g

Block diagram with arrangement of the pre-select switches



Note:

All Q-outputs are open-drain outputs. When used, they must be provided with a resistor (typ. 33 kΩ) to V_{DD}.

Maximum ratings

		Test conditions	Lower limit B	Upper limit A	Unit
Supply voltage	V_{DD}	referred to	−15	0.3	V
Voltage at all inputs except RC-input	V	V_{SS} = 0 V	−15	0.3	V
Storage temperature	T_S		−55	+125	°C
Ambient operating temperature	T_{amb}		0	+70	°C

Operating haracteristics (T_{amb} = 25°C)

Power consumption	P	V_{DD} = −12 V		200	mW
Supply voltage	V_{DD}		−13.5	−10.5	V
L-input voltage	V_{IL}		−15	−8	V
H-input voltage	V_{IH}		−3	0.3	V
Output Q_{VG} (open drain)					
L-output voltage	V_{QLVG}		−13.5	V_{DD}+0.5	V
H-output voltage	V_{QHVG}	$I_Q \leqq 1$ mA	−1		V
Selection-outputs BCD-outputs and carry-output L-output voltage		open drain outputs	−13.5	V_{DD}+0.5	V
H-output voltage		$I_Q \leqq 0.5$ mA	−1		V
Clock input I_T					
Input frequency f_{IT}		when using comparator function (Q_{VG})			
		without divider stage 1:1		10	kHz
		with divider stage 10:1		100	kHz
		with divider stage 100:1		100	kHz
		with divider stage 1000:1		100	kHz
		with divider stage 6000:1		100	kHz
Input frequency f_{IT}		without using comparator function (Q_{VG})		100	kHz

		Lower limit B	Upper limit A	Unit
Pulse width	t_{WIT}	5		µs
HL-transition time	$t_{THL\ IT}$		1	ms
LH-transition time	$t_{TLH\ IT}$		1	ms
Input I_{OSZ} for external oscillator operation				
H-input voltage	$V_{IOSZ\ H}$	−1	0.3	V
L-input voltage	$V_{IOSZ\ L}$	V_{DD}	−8	V
Input frequency	f_{IOSZ}		200	kHz
Pulse width	t_{WIOSZ}	2.5		µs
HL-transition time	$t_{THL\ IOSZ}$		1	µs
LH-transition time	$t_{TLH\ IOSZ}$		1	µs

Description of Functions

1. Correlation of functions common to the counter- and clock-operation

1.1. Programming inputs I_{P1}, I_{P2}, I_{P3}

	I_{P3}	I_{P2}	I_{P1}	Function	
1	H	H	L	Divider 1:1	Counter operation
2	H	L	H	Divider 10:1	Counter operation
3	H	L	L	Divider 100:1	Counter operation
4	L	H	H	Divider 1000:1	Counter operation
5	L	H	L	Divider 6000:1	Counter operation
6	L	L	H	Time base 50 Hz	Clock operation
7	L	L	L	Time base 60 Hz	Clock operation
0	H	H	H	Time base 100 Hz	Clock operation

1.2. BCD Pre-select inputs I_A, I_B, I_C, I_D

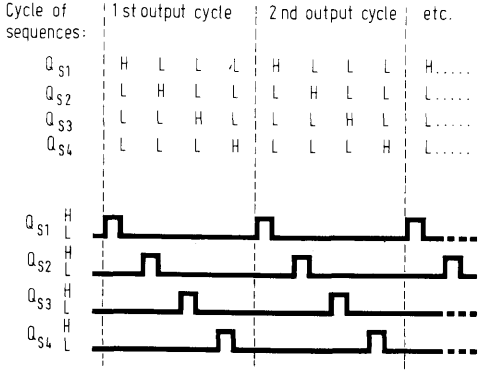
Decimal pre-selection	I_D	I_C	I_B	I_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

1.3. BCD outputs Q_A, Q_B, Q_C, Q_D

Decimal equivalent	Q_D	Q_C	Q_B	Q_A
0	H	H	H	H
1	H	H	H	L
2	H	H	L	H
3	H	H	L	L
4	H	L	H	H
5	H	L	H	L
6	H	L	L	H
7	H	L	L	L
8	L	H	H	H
9	L	H	H	L

1.4. Select-outputs Q_{S1}, Q_{S2}, Q_{S3}, Q_{S4}

The select-outputs have the function of indicating the decimal value of each digit appearing in parallel at the BCD outputs, when the 4 decimal places are put out in series.



Correlation of the H-output voltage $V_{QH\,S1}$ . . . $V_{QH\,S4}$ with the appropriate decimal position at the BCD-output.

	Output decimal position	
	Counting operation	Clock operation
$V_{QH\,S1}$	x 1	x 1 min.
$V_{QH\,S2}$	x 10	x 10 min.
$V_{QH\,S3}$	x 100	x 1 hr.
$V_{QH\,S4}$	x 1000	x 10 hr.

In addition, the select-outputs control the input of the BCD-pre-select data accordingly.

1.5. Clock input I_T

The counter and the divider change their logic condition with the LH transition of the clock signal.

1.6. Oscillator input I_{OSZ}

This input is used for the generation of the cycle-frequency for multiplex operation. As chosen, this frequency can be realized by means of connecting a capacitor (see block diagram) or by applying a clock signal.

(1) Internal oscillator with external *RC*-connection.

For an oscillating frequency of at least 160 kHz the I_{OSZ}-input must be connected to $R = 47\ k\Omega$ and $C = 33$ pF. By changing C (20 . . . 100 pF) and R (20 kΩ . . . 100 kΩ) the cycle frequency can be changed within a range of 100 . . . 500 kHz. When using the comparator function at $f_{IT} \leqq 1$ kHz, resistance R is not required.

(2) External oscillator for the synchronous operation of several SAJ 341 A circuits.
The oscillator frequency must be 16 times higher than the maximum clock input frequency occurring.

2. Counter operation

When the programming inputs are connected according to table 1.1, positions 1 through 5, this circuit operates as a decade-counter exclusively.
At 1, the counting pulses from clock input I_T move directly into the 4-decade counter (10^0, 10^1, 10^2, 10^3). The contents of this counter is periodically put out through the multiplexer.
At 2 through 5, the corresponding divider is connected ahead of the 4-decade counter. Thereby the input clock pulses are additionally divided by 10, 100, 1000 or 6000.

2.1. Clock blocking inputs I_B

By applying an H-signal at the clock blocking input, the input of pulses can be inhibited; Q_{VG} is on an L-potential during this time. If a blocking signal U_{IHB} occurs during the clock voltage V_{ILT}, the LH-transition of the blocking signal is still counted.

2.2. Comparator output Q_{VG}

When the 4-decade counter reaches the number pre-selected through the BCD-pre-select inputs, the comparator output supplies an H-signal.

2.3 Additional programming input I_{ZP}

Table of functions:

L at I_{ZP}	When the 4-decade counter reaches the pre-selected number, an H-signal appears at the comparator output Q_{VG}, which changes back to L with the next decade-counter clock pulse. Counting is continued.
H at I_{ZP}	When the pre-selected number is reached, Q_{VG} changes to H. Circuit-internally blocking of the clock occurs, i. e. the counter remains on the pre-programmed count and Q_{VG} equally remains on an H-potential.

2.4. Carry output $Q_{Ü}$

The carry output $Q_{Ü}$ makes it possible to connect several SAJ 341 A circuits in series, thereby increasing the counting capacity.
$Q_{Ü}$ assumes an L-potential at a count of 8000 and supplies an LH-transition and hence a carry signal when changing from 9999 to 0000.

2.5. Reset input I_R

Counter and divider are reset to zero when an L-signal is applied to reset input I_R. The reset signal is dominating, i. e. no clock pulse is counted as long as a signal is active at I_R.

3. Clock operation

In connection with programming inputs 6, 7 and 0 (see 1.1.) the SAJ 341 A operates as a digital clock with an output of minutes and hours. Depending on the connection of the programming inputs, the clock input may be operated with a time reference frequency of 50 Hz, 60 Hz or 100 Hz.

3.1. Possibility of time-setting

Clock operation is possible with or without use of pre-select switches, which makes possible several ways of time-setting.

3.1.1. Connection of the pre-select inputs to a pre-select switch

Using the pre-select switch can provide 2 functions:

(1) Using a key-contact at reset input I_R, the clock can be set to a pre-selected time by applying a short L-signal (HL-transition).

(2) Additionally, the clock can perform a switching function (e. g. sound an alarm) if provision is made that, upon reaching the pre-selected time, an H-signal is present at comparator output Q_{VG} for 1 minute (provided that the pre-select setting is not changed during the H-signal).

3.1.2. Operation without pre-select switch

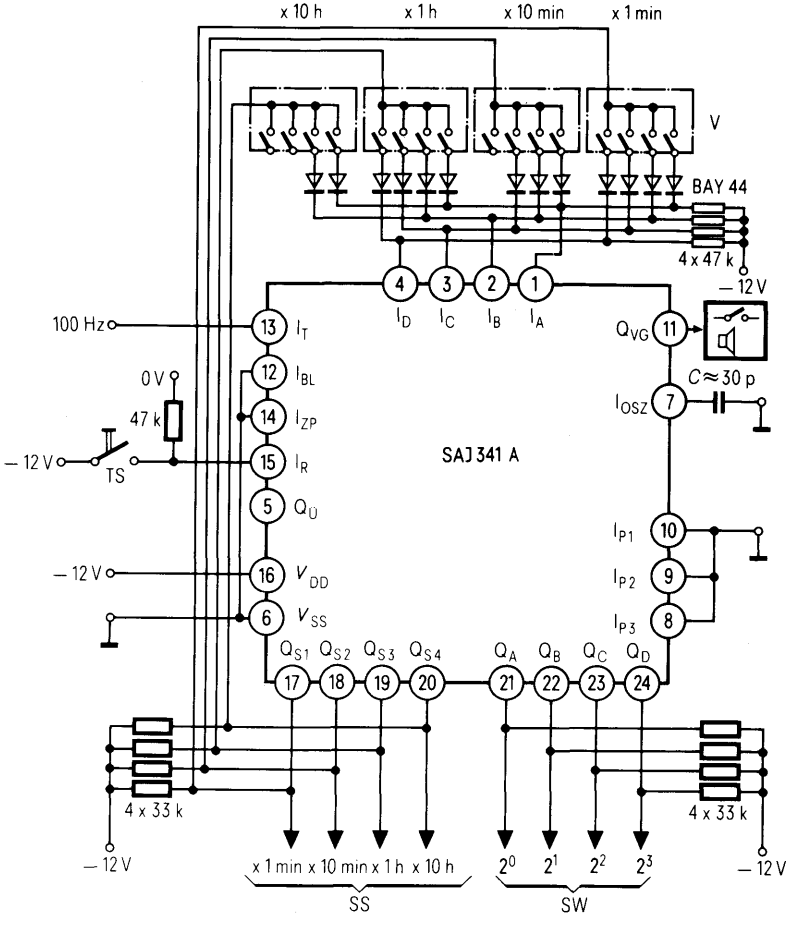
All pre-select inputs are to be provided with an L-signal (V_{DD}). By connecting inputs I_{ZP} and I_B with bounce-free keys, minute- and hour-counters can be set.
By applying an L-signal (HL-transition), single pulses can be applied through I_{ZP} to the hour-counter and through I_B to the minute-counter. A defined output position is achieved by turning-on the mains voltage or by applying a reset signal to I_R (see also 2.5). For a proper setting, the clock signal should be interrupted during this time.

3.2. Carry output $Q_{Ü}$

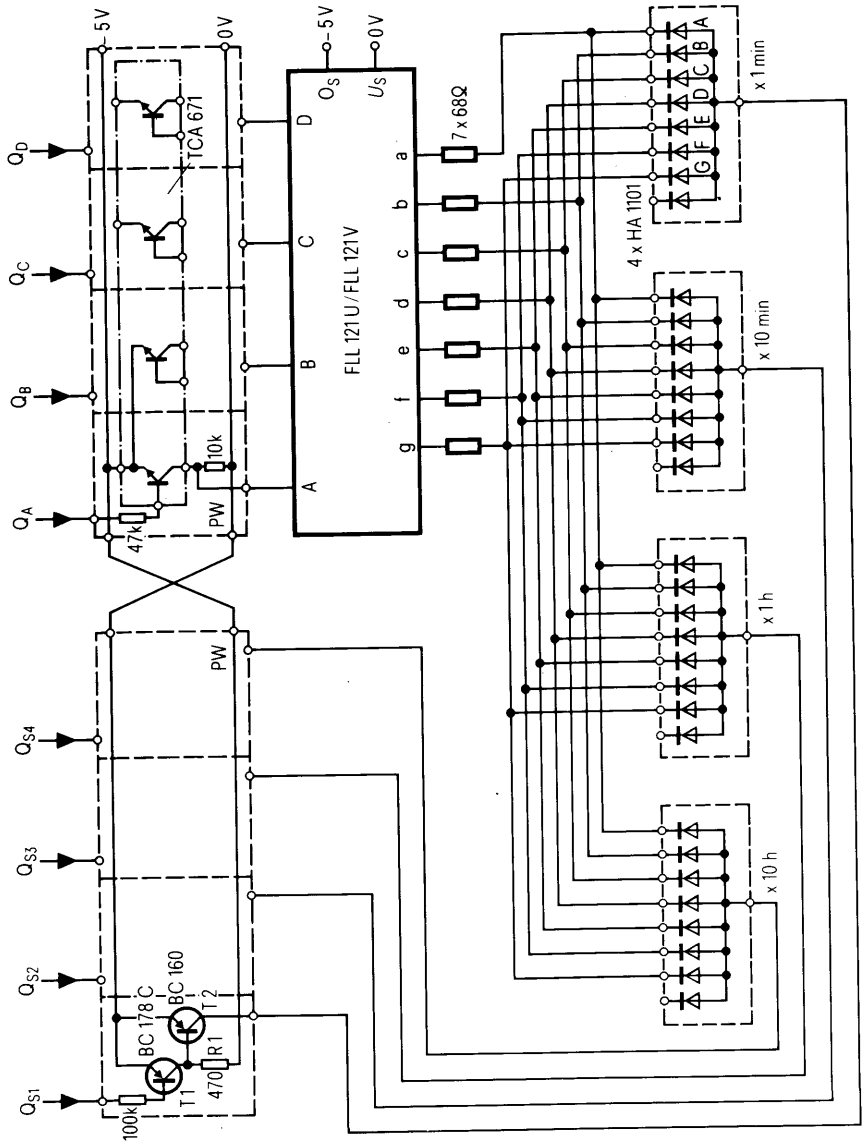
The output $Q_{Ü}$ supplies a day-carry by turning to an L-potential at 20.00 o'clock and by providing an LH-transition when changing from 23.59 to 0 hours; this transition can be used to drive an additional SAJ 341 A, for example.

Application examples

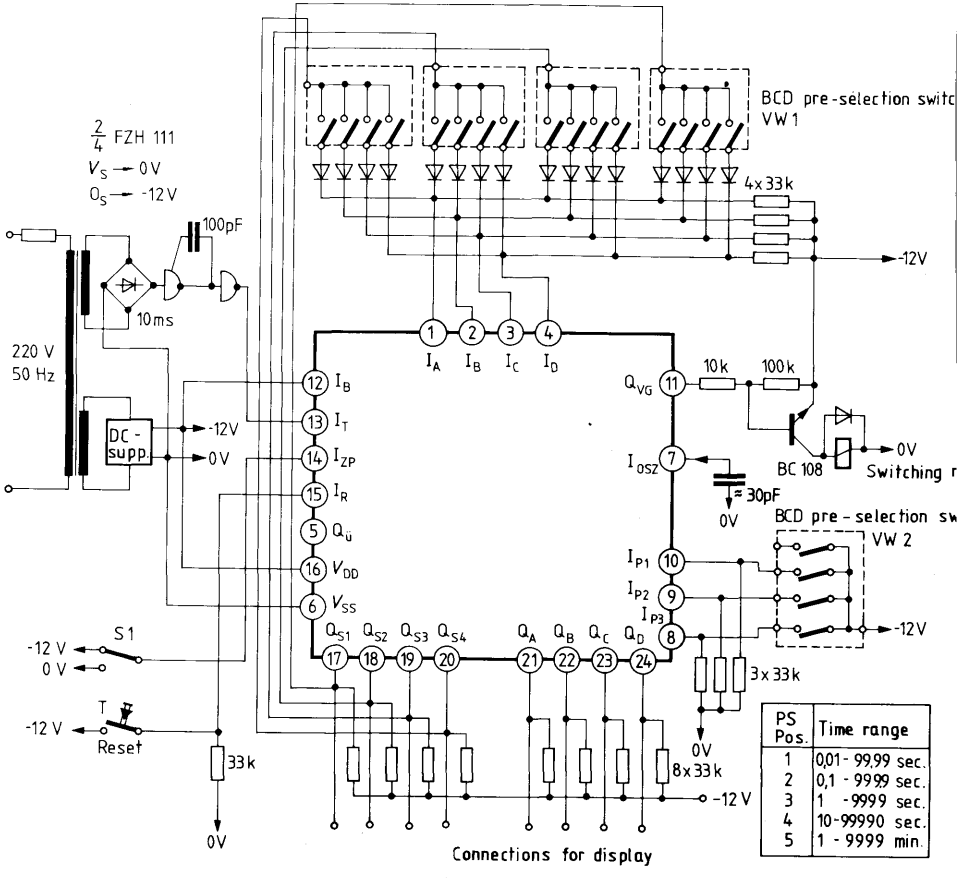
Connection of the SAJ 341 A for a clock with pre-selection of the time to be set and possibilities for setting a switching- or alarmtime.



Interface circuit for the SAJ 341 A for a clock with LED-display



Digital timing circuit
(timing range 10 ms . . . 9999 min.)



PS Pos.	Time range
1	0,01 - 99,99 sec.
2	0,1 - 9999 sec.
3	1 - 9999 sec.
4	10 - 99990 sec.
5	1 - 9999 min.

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